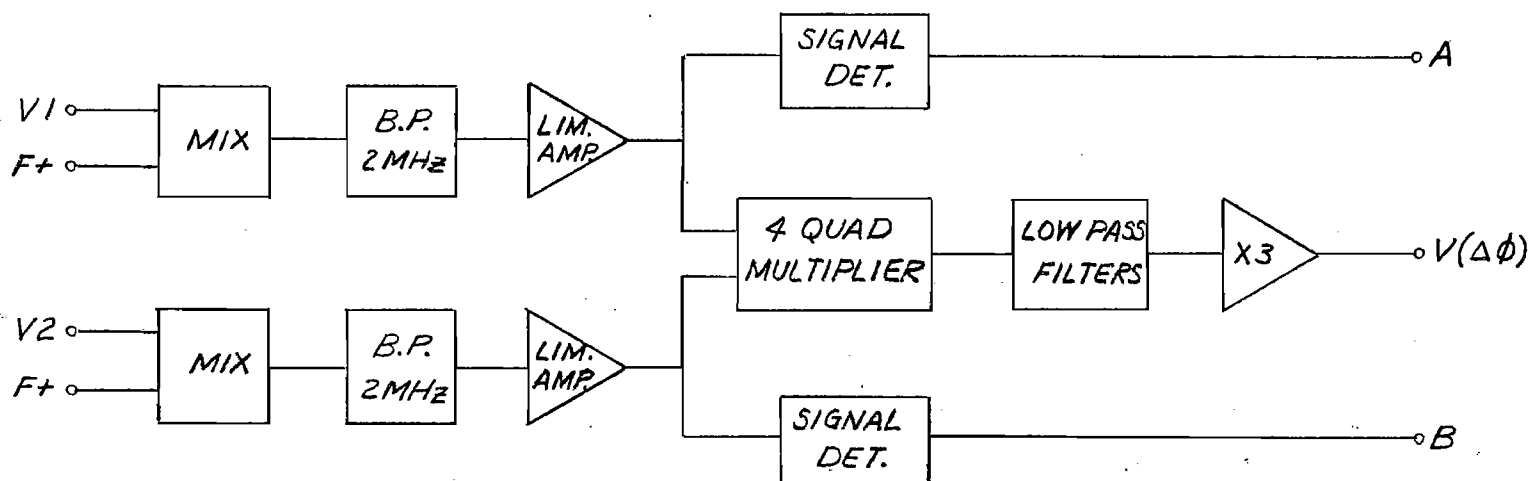


Phase Detection

The following scheme seems to be the preferred method of phase detection.



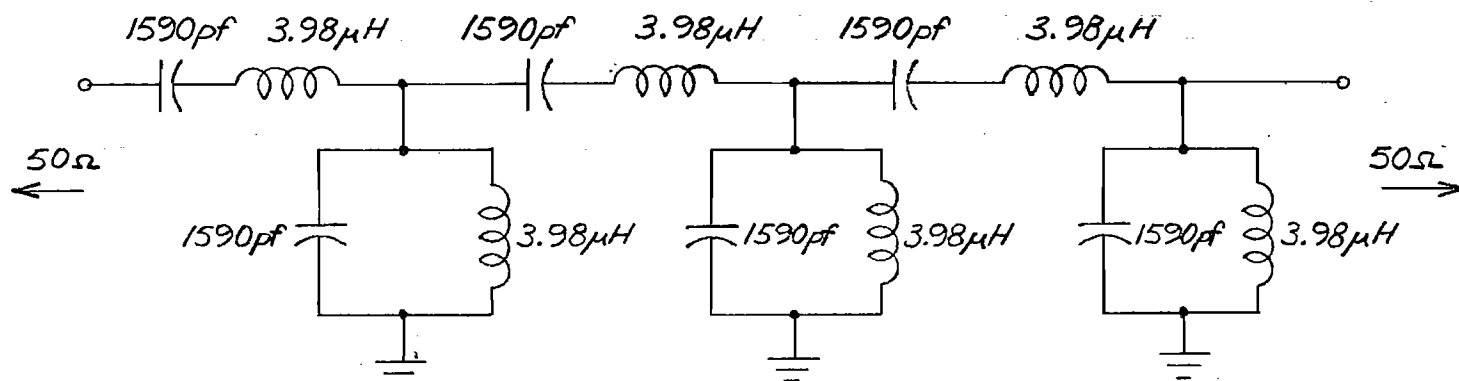
V_1 and V_2 are two signals whose $\Delta\phi$ is to be measured. $F+$ is a sideband shifted 2 MHz in frequency, provided by the synthesizer.

A and B are logic outputs indicating the presence or absence of RF in the two channels. $V(\Delta\phi)$ is a linear function of $\Delta\phi$. $V(\Delta\phi)$ is not a function of the amplitudes of V_1 or V_2 over a 1000:1 range.

This note will describe the various components of the system, their important features, overall system performance, and possible problems.

Band Pass Filters

These are 10 element constant K bandpass filters shown below



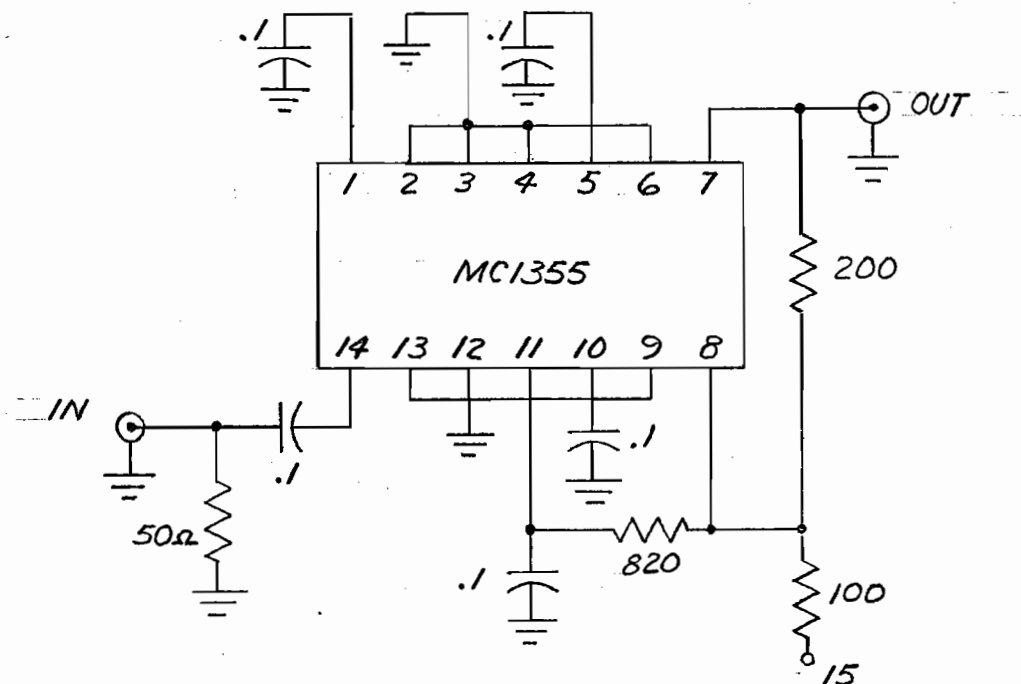
Frequency characteristics are shown in Graph #1.

Construction of the filters is of particular importance. The filters are to be constructed in pairs inside small aluminum boxes to be clipped onto the PC board. Ceramic capacitors and toroidal inductors (13 turns of #32 wire wound on F2062-1-Q1 $\mu=125$). 10% accuracy components are fine (this is reflected in the not-so-ideal frequency characteristics), but mounting of each detector's pair of filters in close physical proximity is very important for temperature stability. We measured the $\Delta\phi$ introduced by a pair of filters as they were heated from 25°C to 45°C to be less than $1\frac{1}{2}^\circ$, so in operation, this source of error should be negligible.

Cross-talk between filters was measured to be -60 dB ($V_{1out}=10^{-3}V_{2in}$). This sounds pretty good, yet with the limiting amps having a gain of 60 dB, erroneous operation is conceivable if one signal is lost, and the other is at a high level. The conclusion is to not drive the mixers higher than is necessary for their proper operation.

Limiting Amplifiers

These are MC1355's in the following circuit.



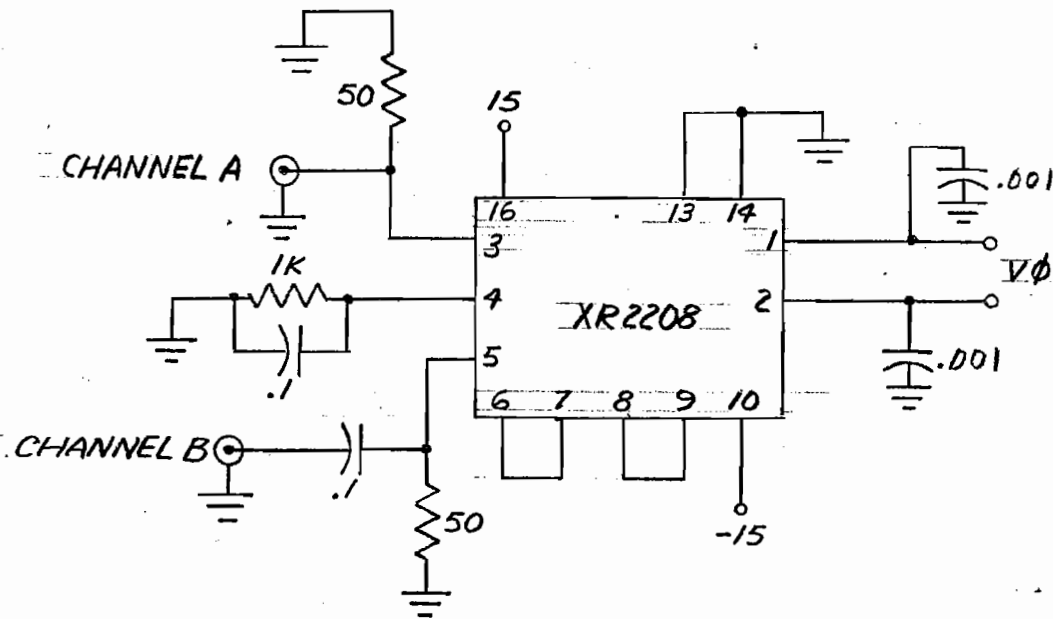
The output is a high quality square wave of .2 volts p-p, over a very wide input amplitude range. Below an input of around 250 μ V limiting does not take place, and the output is sinusoidal. Phase shift is small throughout the range, as shown in Table #1. (In this data the chip was followed by a class A Mosfet amp.) Above 80 mv, no amplitude dependence is observed, except when the chip is overdriven. For a chip supply voltage of 15 V, overdriving takes place at around 2 volts RMS. The chip is not sensitive to temperature change.

Table 1. Phase characteristics of MC1355
as function of input amplitude.

V_{in}	V_{out}	$\Delta\phi$
	(rms)	
80 mv	5.2 v	-6.0°
70	5.2	-6.2
60	5.2	-6.4
50	5.2	-6.4
40	5.2	-6.4
30	5.2	-6.2
20	5.2	-6.4
10	5.3	-6.5
9	5.3	-6.6
8	5.3	-6.7
7	5.3	-6.9
6	5.3	-7.2
5	5.3	-7.5
4	5.3	-7.9
3	5.3	-8.5
2	5.3	-8.9
1	5.3	-9.6
.9	5.3	-9.6
.8	5.3	-9.6
.7	5.2	-9.6
.6	5.2	-9.4
.5	5.2	-9.1
.4	5.2	-8.5
.3	5.1	-7.5
.2	4.8	-5.8

The Multiplier & Output Filter

The square wave outputs go to an XR-2208 4 quadrant multiplier in the following circuit:



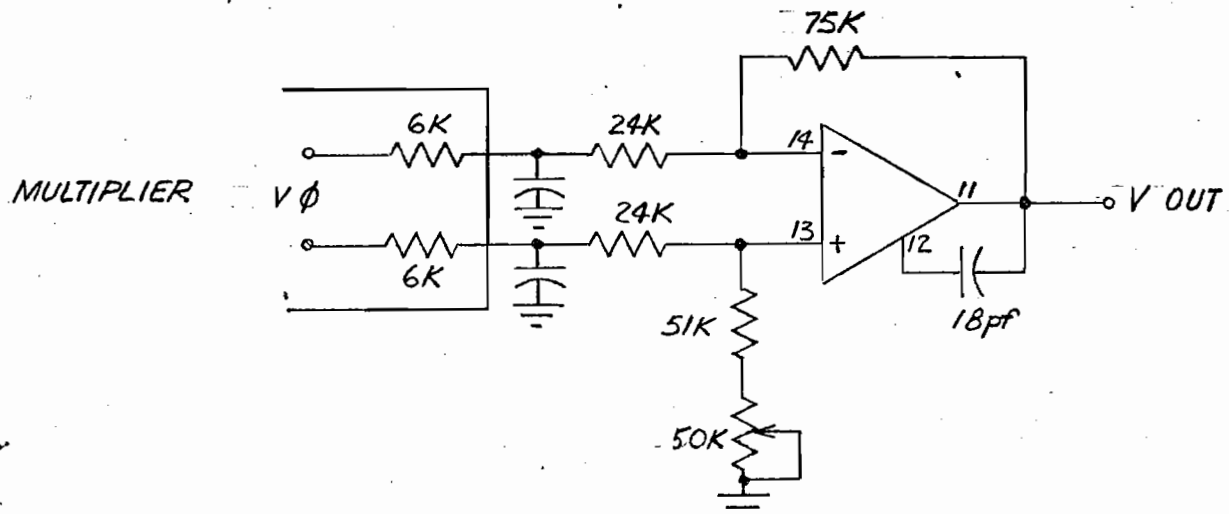
The internal resistance at pins 1 and 2 is approximately 6K, so that the two capacitors at pins 1 and 2 complete low pass filters of time constant around 10^{-5} sec., and for 2 MHz square waves

$$V_d = K(\Delta\phi - 90^\circ)$$

K can be adjusted externally. In this circuit we have maximised it by shorting 6-7 and 8-9. $K \approx .04$ volts/degree

Output Op Amp

The XR 2208 comes with an internal op amp, which we use to vary the gain of the total system and zero the output.



Assuming the trim pot is set around 24 K, the gain of this differential configuration will be 3, which results in an overall system response of

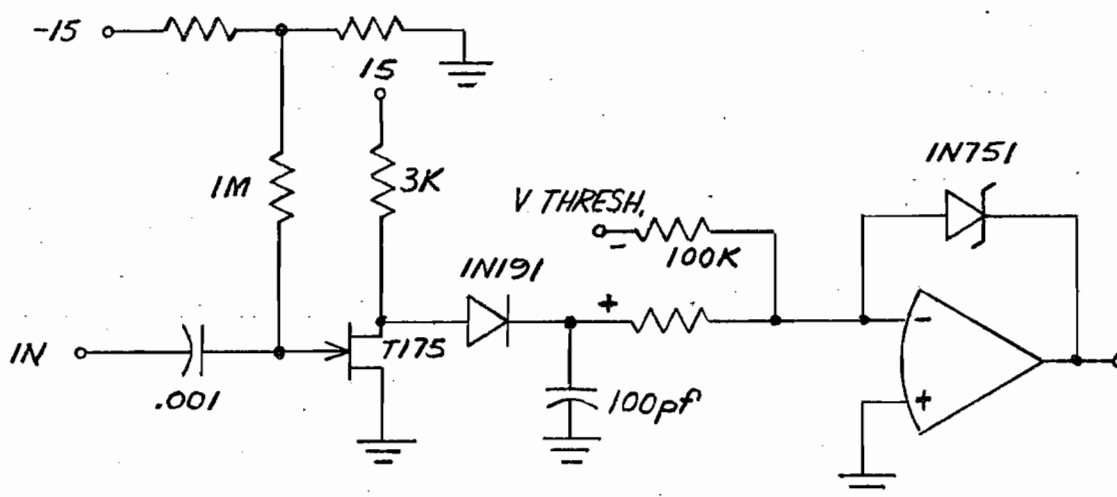
$$V_{out} = .116(\Delta\phi - 90)$$

Clearly this gain is easily adjustable, and may well change if desired. The trim pot is used to zero the output, given two known 2 MHz signals (sine or square) exactly 90° out of phase. This one adjustment should suffice to compensate for all error introduced in the filter and chip output offsets.

The multiplier chip was also observed to be insensitive to temperature drift. Specifications quote a typical temperature drift of .5 mV/°C, or 1/20 of a degree per 10°C.

Signal Detection

The following circuit gives a logic output zero if RF of amplitude greater than 150 mv p-p, logic 1 if the signal drops below that.



This circuit has the necessary virtue of not loading the limiting amps, and it has an adjustable threshold. Logic level can be selected with the Zener.

Mixers

We used the mixers described in RF #28 in testing the circuit. It is found that these mixers introduce an amplitude dependent phase distortion considerably worse than the detection circuit itself, on the order of a few degrees. We are presently testing different mixers for better performance, in case the present mixers are not deemed good enough.

Circuit Performance

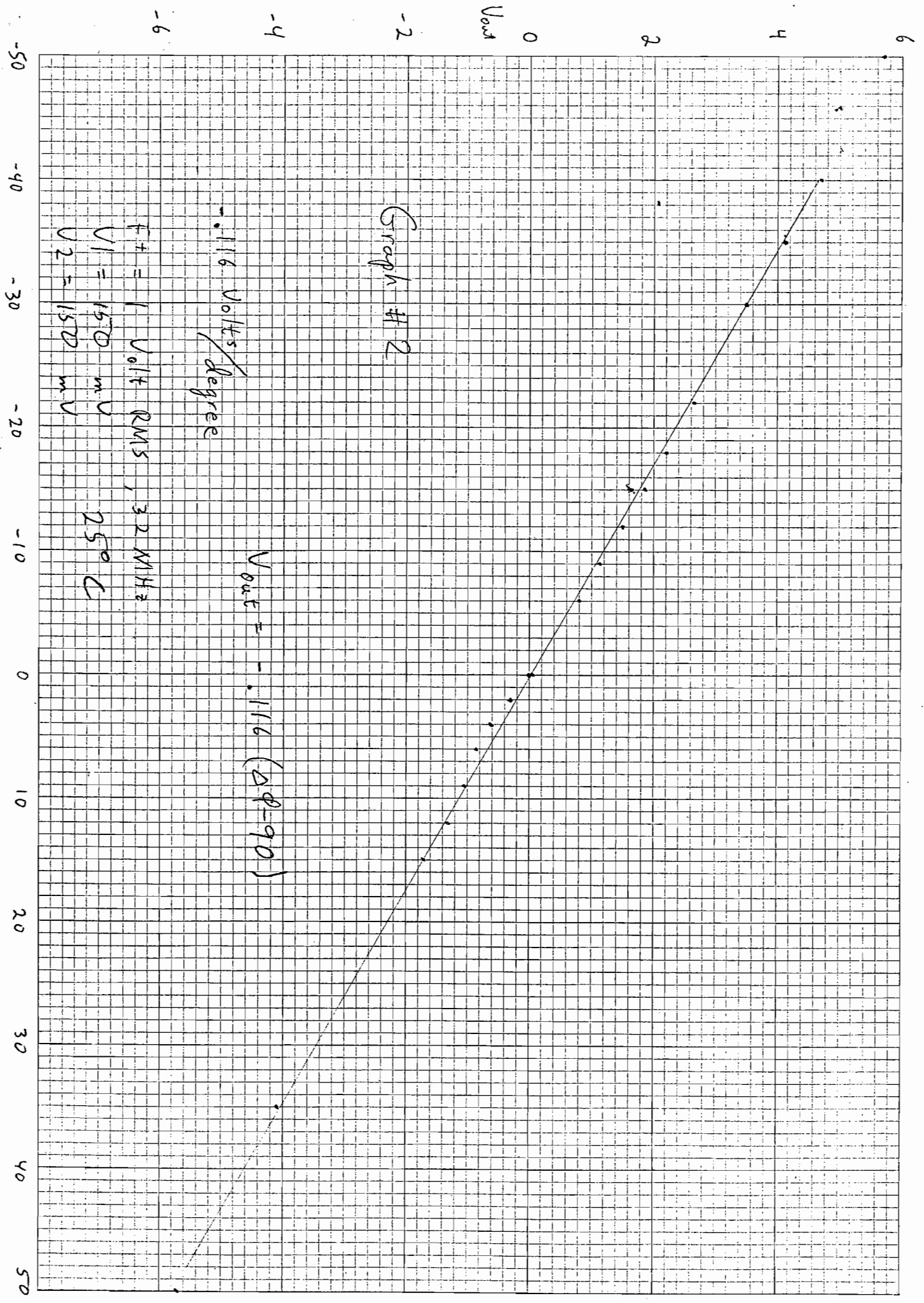
Graphs #2 and #3 show V_{out} as a fn of $\Delta\phi$ for the given parameters. Different driving levels exhibited exactly the same $-.116$ volts per degree constant.

Graph #4 shows equivalent degree error as one limiting amp input varies from 1 mV to 500 mVRMs, while the other input is held at 500 mVRMs. This situation will be important in low level testing. Notice also that 2 MHz V_1 and V_2 are used i.e., no mixer error is involved. Above 5 mV, the maximum error is $1\ 1/2^\circ$.

Graph #5 shows equivalent degree error as both V_1 and V_2 (inputs to limiting amps. Here again no mixing is involved) are varied together at a high level. The abscissa is the magnitude (peak to peak) of $V_1=V_2$. The left ordinate is the voltage output (V_1 and V_2 are 2 MHz, 90° out of phase). The right ordinate shows equivalent degree error. Over the range 10 mV to 10 V (3.5 mV RMS to 3.5 VRMs) maximum error is $.8^\circ$.

Graphs # 6 & #7 show the frequency response of the phase detector. To make this measurement we used the phase shifter (RF#34) followed by our phase detector. Once again, all RF is at 2 MHz, so no mixing is involved. The top curve is the shifter alone, from RF34, the bottom curve is the combination; consequently the phase detector amplitude and phase response is the difference. This is shown on Graphs #8 and #9. Thus the phase detector has a frequency response of around 35 kHz.

$\Delta\phi = 90$

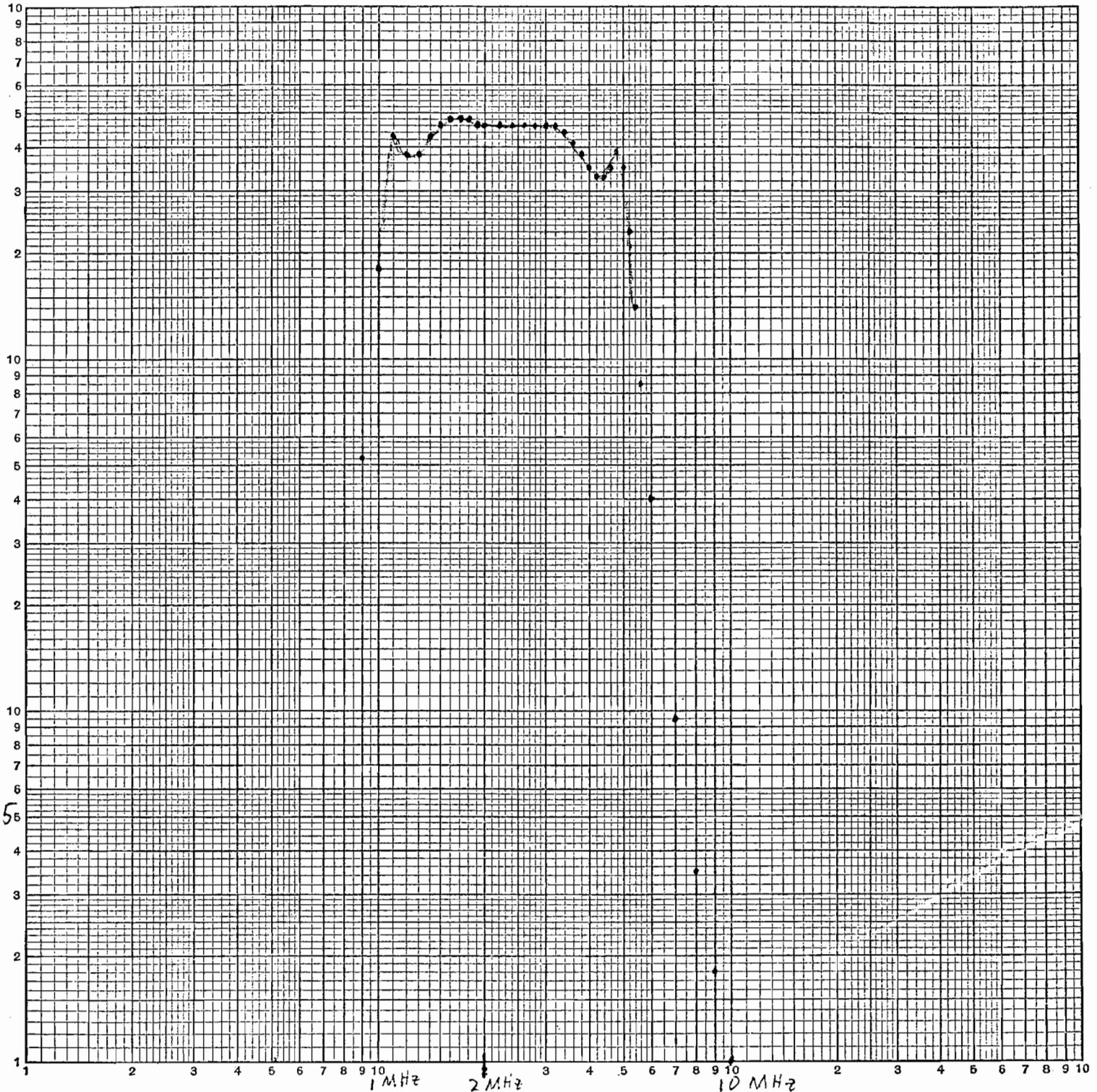


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mV

2 mV



2 MHz Band Pass Filter
Amplitude Characteristics.

Graph #1

$V_{in} = 50 \text{ mV}$

$\Delta \phi - 90^\circ$

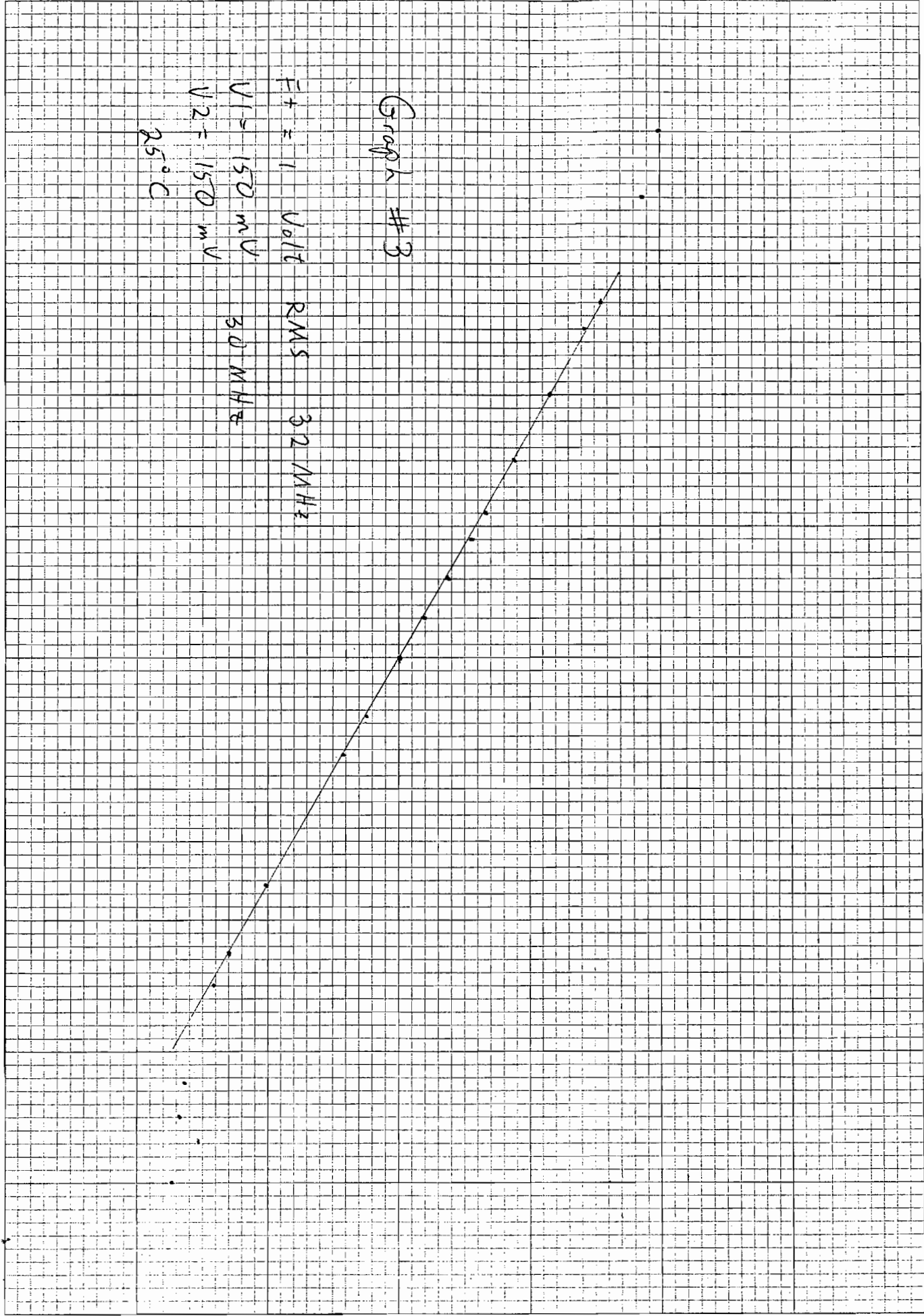
Graph #3

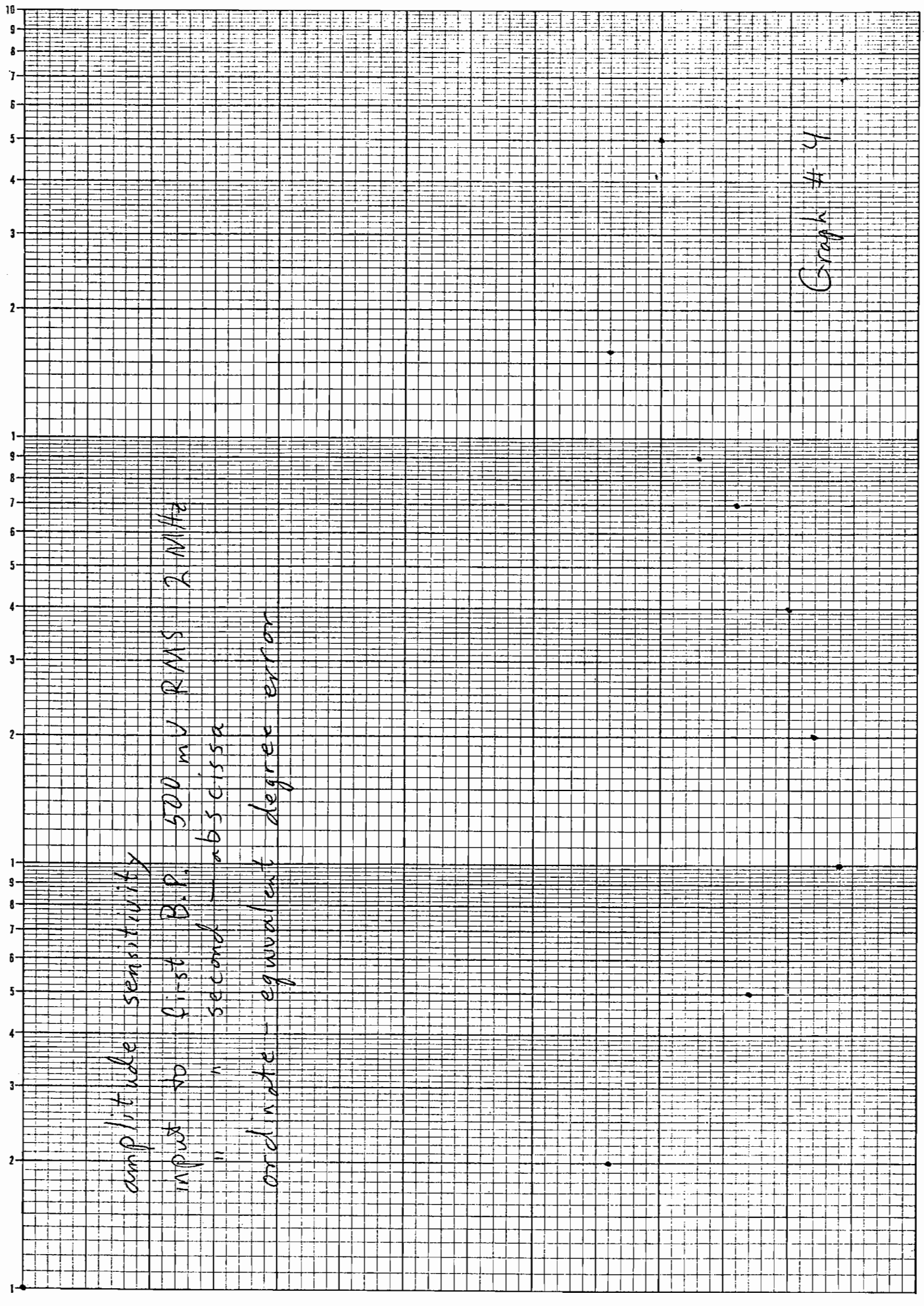
$F = 1$ Volt RMS 32 MHz

$V_1 = 150$ mV 30 MHz

$V_2 = 150$ mV

25°C





amplitude sensitivity

input to first B.P. 500 mV RMS 2 MHz

" " second abscissa

ordinate - equivalent degree error

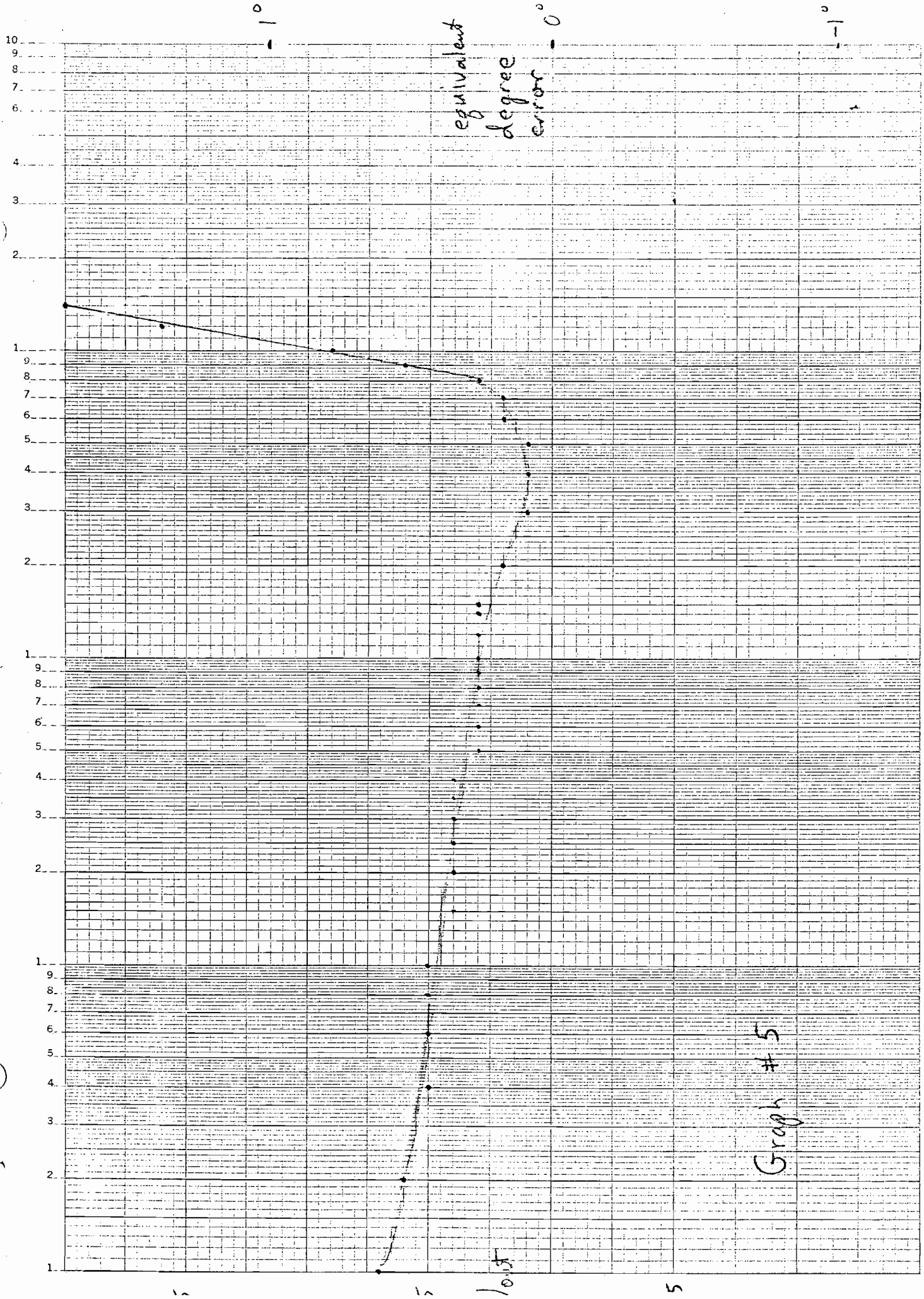
100 mV

10 mV

1 mV

46 6010

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Graph #5

10V

1V

P-P

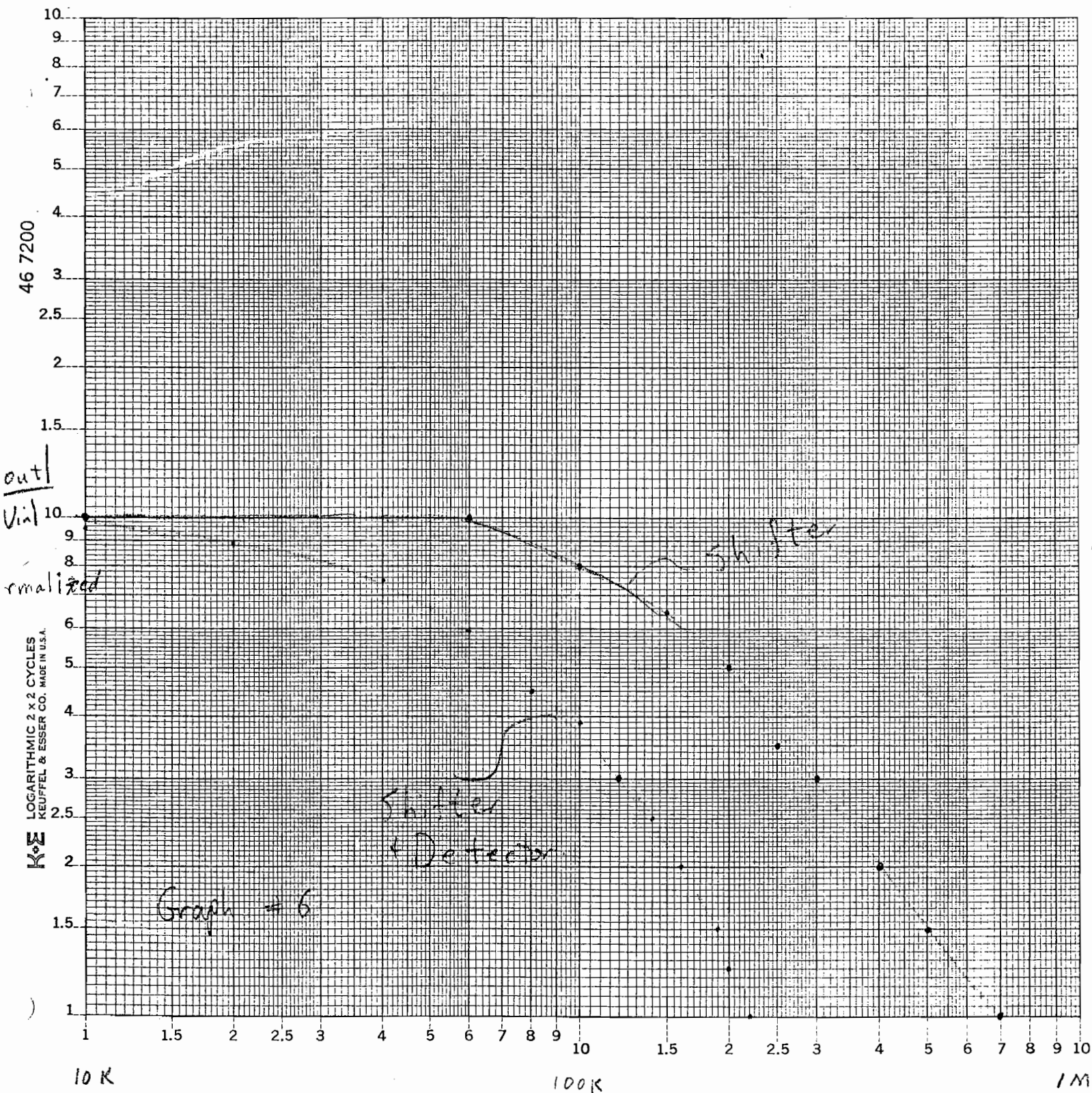
100mV

$|V_1| = |V_2|$

2MHz

$\phi = 90^\circ$

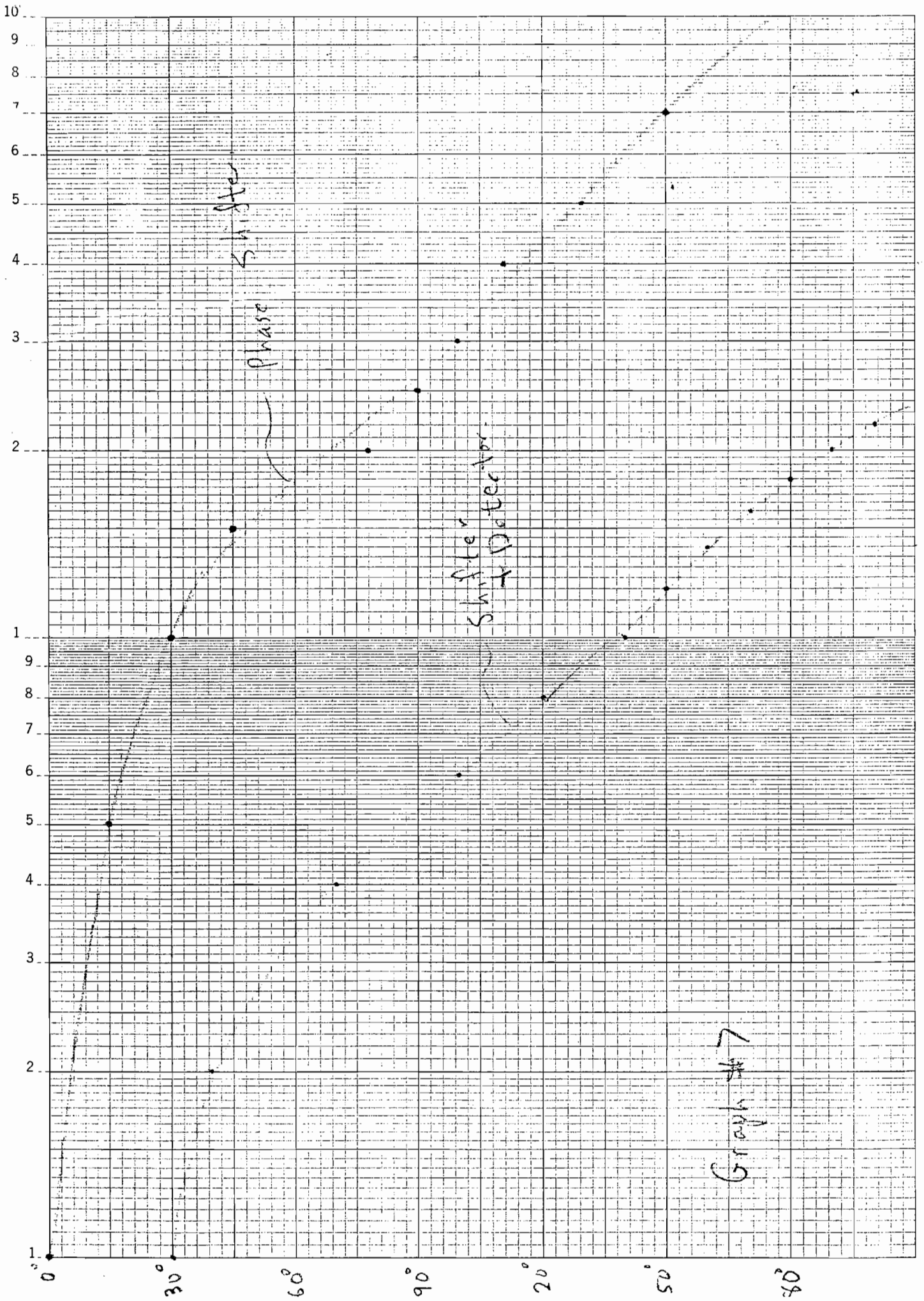
10mV



Fast Phase Shifter
Frequency Response

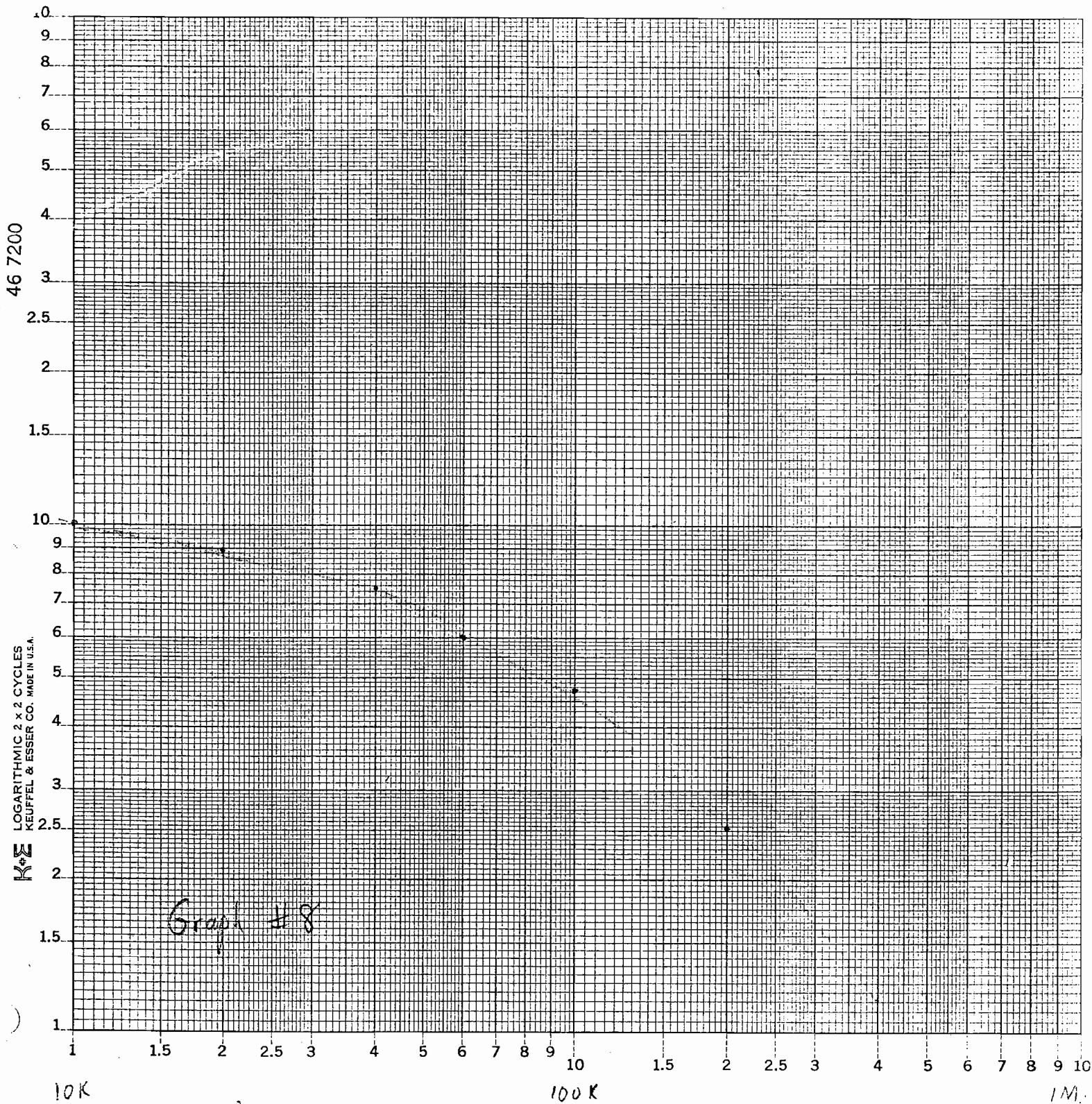
Phase Shifter + Detector
Frequency Response.

(1 1 1 0)



Graph #7

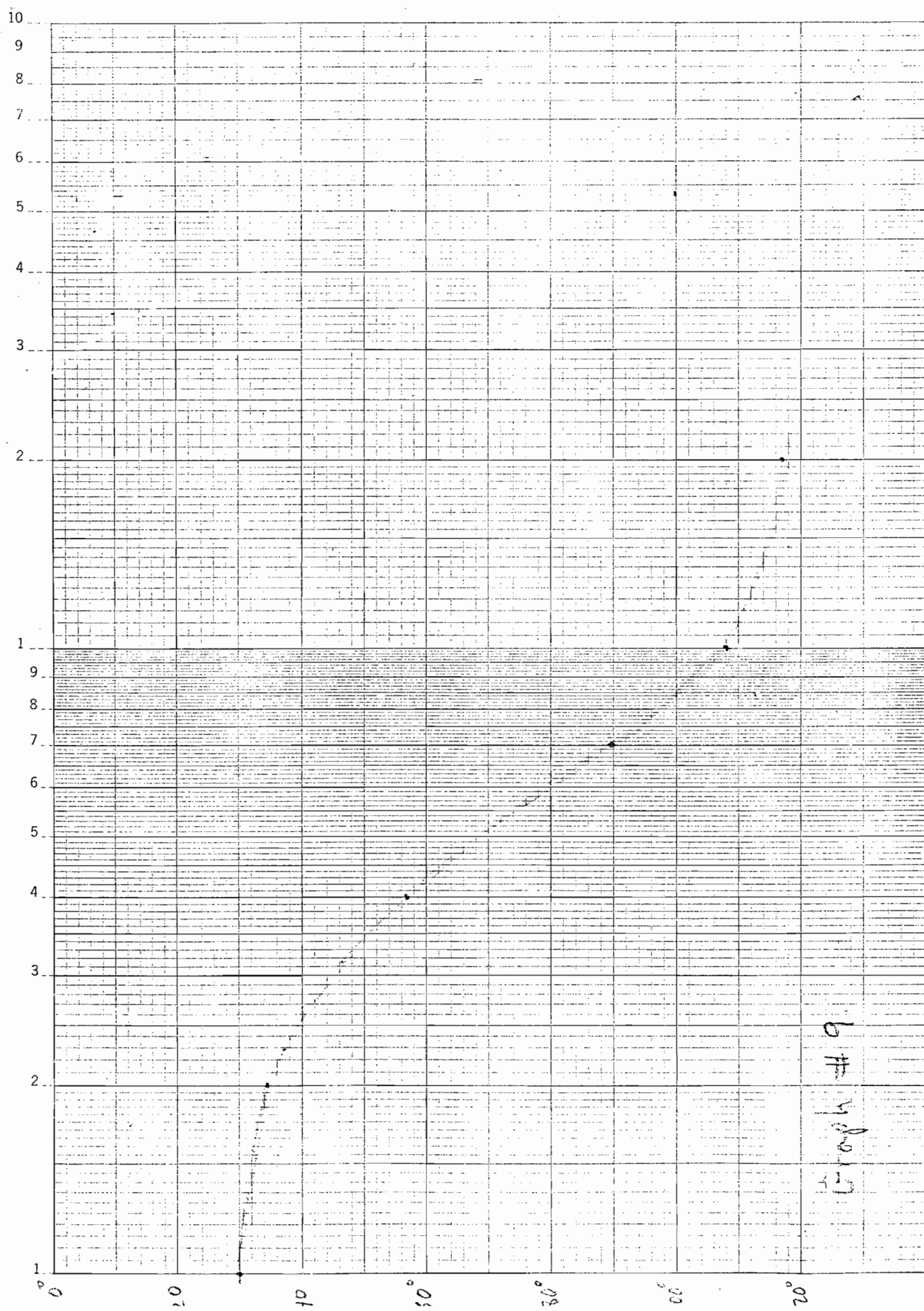
10K Phase Shifter, Phase Shifter + Detector Phase Freq. Response (Phase)



Phase Detector Frequency Response
(Amplitude)

46 4972

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Graph #9

10kHz Phase Detector Frequency Response (Phase) 100kHz