214-0103-01-01_00

R.F. Note #102

J. Vincent
Oct. 16, 1985

Contents:

1. Neutralizing the K500 and K800 dee to dee capacities.

RF Note #96 summarizes the reasons to pursue an advancement in our neutralizing methods. The purpose of this note is to investigate this problem in detail and to present some alternate approaches. The goal is a set of mechanical parameters which will increase the sparking thesholds we now experience and allow us to completely nuetralize over our entire operating band of 9 to 27 Mhz. The analysis begins assuming the perferred method to be stationary loops whose capture area remains perpendicular to the applied rf magnetic field. This approach may prove to be impractical, but it is worth a try.

2. Sparking

I will attempt to present a design which maintains gradients and clearences which should not spark with needle gap type geometries. The absolute worst case would occur at 9 Mhz. where 100 KV peak on the dee yields 90 KV peak at the neutralizing loop locations. At standard temperature and pressure the required needle gap to maintain this potential comes from the equation:

$$L = (3.82\times10^{-2})\times VPEAK - (2.94\times10^{-2}) \text{ inches}$$

For our case L = 3.4 inches. Since we only have 5 inches available, this approach is not practical. From a chart in the control room, I see the maximum necessary dee voltage as a function of frequency approximately obeys:

$$Vdee = 4.61F + 8.64 \text{ KV} \qquad 9 < F < 21 \text{ Mhz.}$$

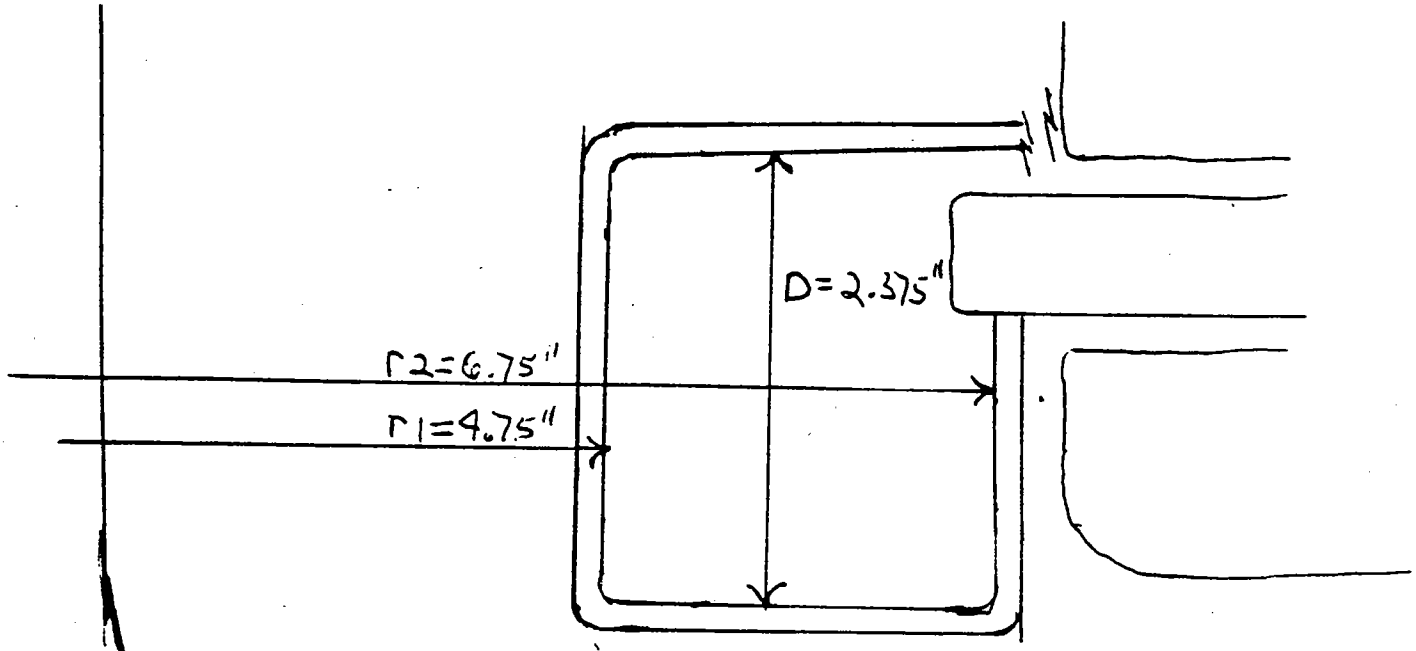
$$Vdee = 100 \text{ KV} \qquad F > 21 \text{ Mhz.}$$

A table of Vloop vs. Vdee as a function of frequency is now helpful.

F(Mhz)	Vdee(KVpeak)	Vloop(KVpeak)
9	50	45.0
11	59	51.5
13	69	57.5
15	78	61.5
17	87	63.9
19	96	65.6
21	100	62.5
23	100	56.6
25	100	50.0

So it appears that the worst case occurs somewhere between 17 and 19 Mhz at which time the voltage at the loops reaches a maximum value of about 66 KV. Now L = 2.46 inches for a needle gap.

This leaves the following absolute maximum dimensions for the loop:



Absolute Maximum Allowable Loop

Corona ring.

3. Loop Size .

I wish to hold the loop voltage to 1 KV peak or less. Having choosen the above number, the loop dimensions may now be calculated.

$$VL = -d\Psi/dt \quad ; \text{where} \quad \Psi = \int B\, dS$$

$$\Psi = (\mu I/2\pi) \int_{r1}^{r2} \int_{0}^{D} (1/r)\, dz dr = (\mu I D/2\pi) \ln(r2/r1)$$

$$|VL| = \mu I F D \ln(r2/r1)$$

To greatly simplify this, I demand the loop be square, hence;

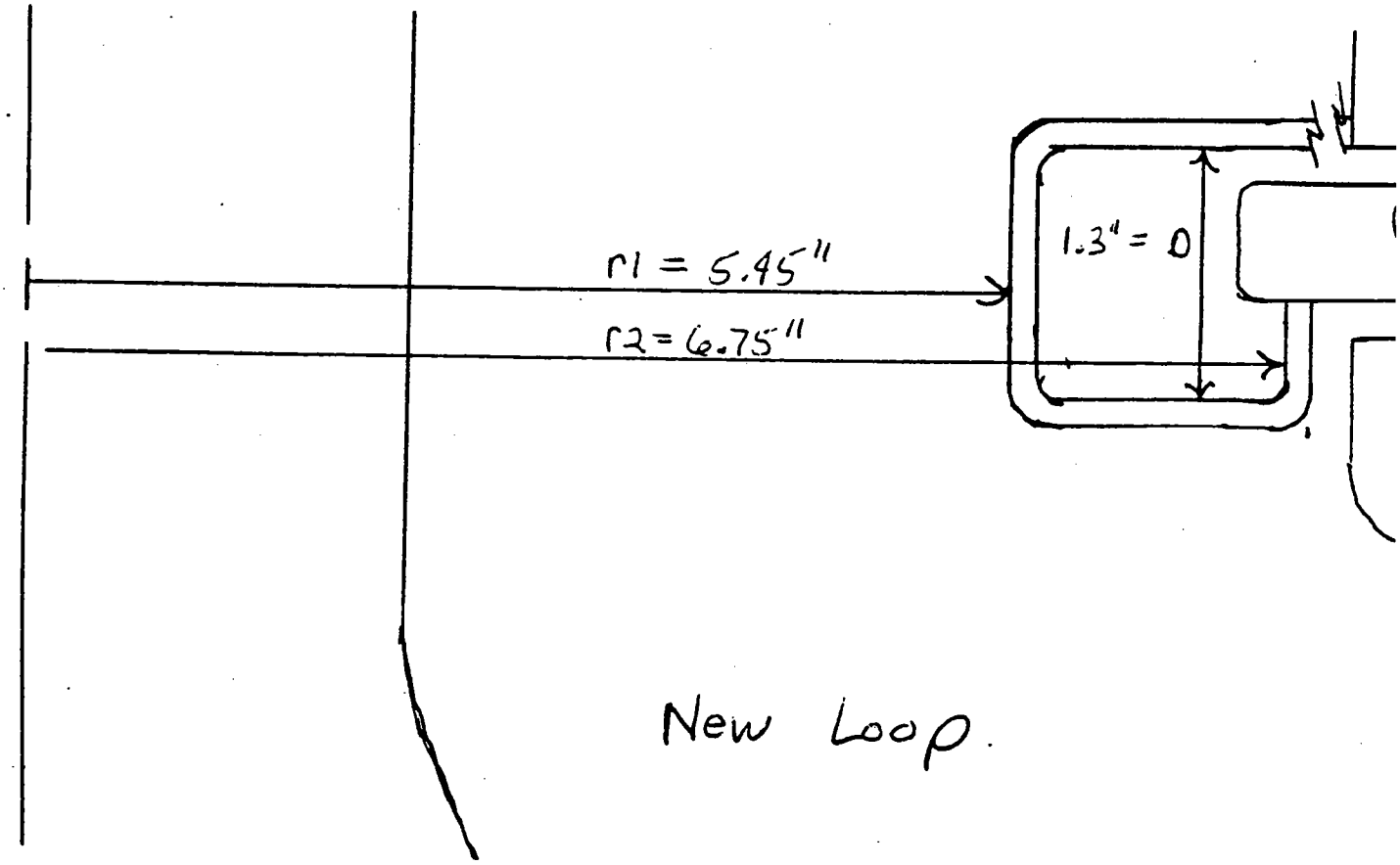
$$D = r2 - r1$$

since: r2 = 6.75 inches and VL(max) = 707 Volts rms

, and $(r2 - r1) \ln(r2/r1) = VL(max)/(\mu I F)$;

r1 and D may now be calculated.

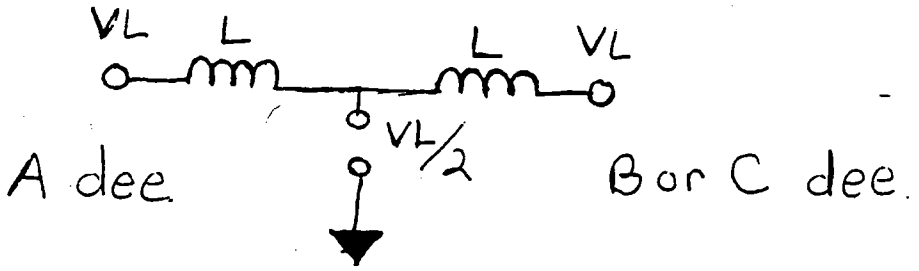
The maximum current and frequency occur concurrently at 27 Mhz where the current is 2960 Amps rms. D is found to be 1.3 inches and r1 is 5.45 inches. The new geometry to contend with is now shown:



New Loop.

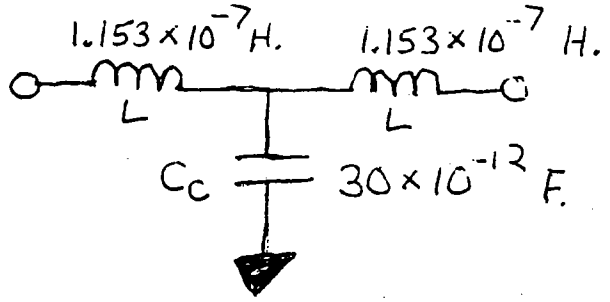
4. Current K500 Condition

RF Note #79 stated the A to B capacitance was .2 pf, while the A to C capacitance was .15 pf. This has reversed itself somehow, since A to C is now greater than A to B. We can infer what the values of capacitance are now from K500 data. The following table lists nuetralizing circuit conditions when the A dee was excited. The A to B and A to C nuetralizing circuit voltages were measured at VL/2 in the following electrical equivalent schematic at 20 KV dee peak. This data has been adjusted for 100 KV dee peak.



F(Mhz)	VL(A to B, volts rms)	VL(A to C, volts rms)
9.310	400	480
16.094	720	1050

The measured value of the self inductance of one of our loops is about 1.153×10^{-7} Henrys. This inductance is not constant however, due to the coupling from one loop to another. The circuit looks like:



I am modeling the connecting transmission line as a lumped 30 pf capacitor to common. Now the inductance of the nuetralizing system is not simply 2L, but one can easily verify it is:

$$Leg = L[1+1/(1-\omega^2 LCc)]$$

F(Mhz)	Leq
9.310	2.32×10^{-7}
16.094	2.35×10^{-7}

By now relating the stored electric and magnetic energys. the dee to dee capacitances may be inferred.

$$U_H = (1/2) L I^2_{rms} = (1/2Leq)(VL/\omega)^2$$

We have two nuetralizing systems per resonator, hence;

$$U_H = (1/Leq)(VL/\omega)^2$$

The electric stored energy is:

$$U_E = (1/4) C V^2_{deepeak}$$

then,

$$C = (4/Leq)(VL/Vdee\omega)^2$$

The next table lists the results:

F(Mhz)	C(A to B)	C(A to C)
9.310	.0863pf	------
16.094	.0863pf	.184pf

Why the dasn for C(A to C) at 9.310 Mhz?

Because we can't nuetralize A to C at 9 Mhz.

Whether these numbers are totally accurate or not doesn't matter. Since they do predict what is going on now. consistancy will allow us to design better.

The next step necessary to check all this. is to verify the stem currents in this location calculated by SF08 and Superfish. This will be done by comparing the measured loop voltages to the calculated values. The follow pots on our loop systems change 8 volts for a 70 degree angular rotation.

The loop voltage comes from:

$$|VL| = \mu IFD\cos\theta \ln(r2/r1)$$

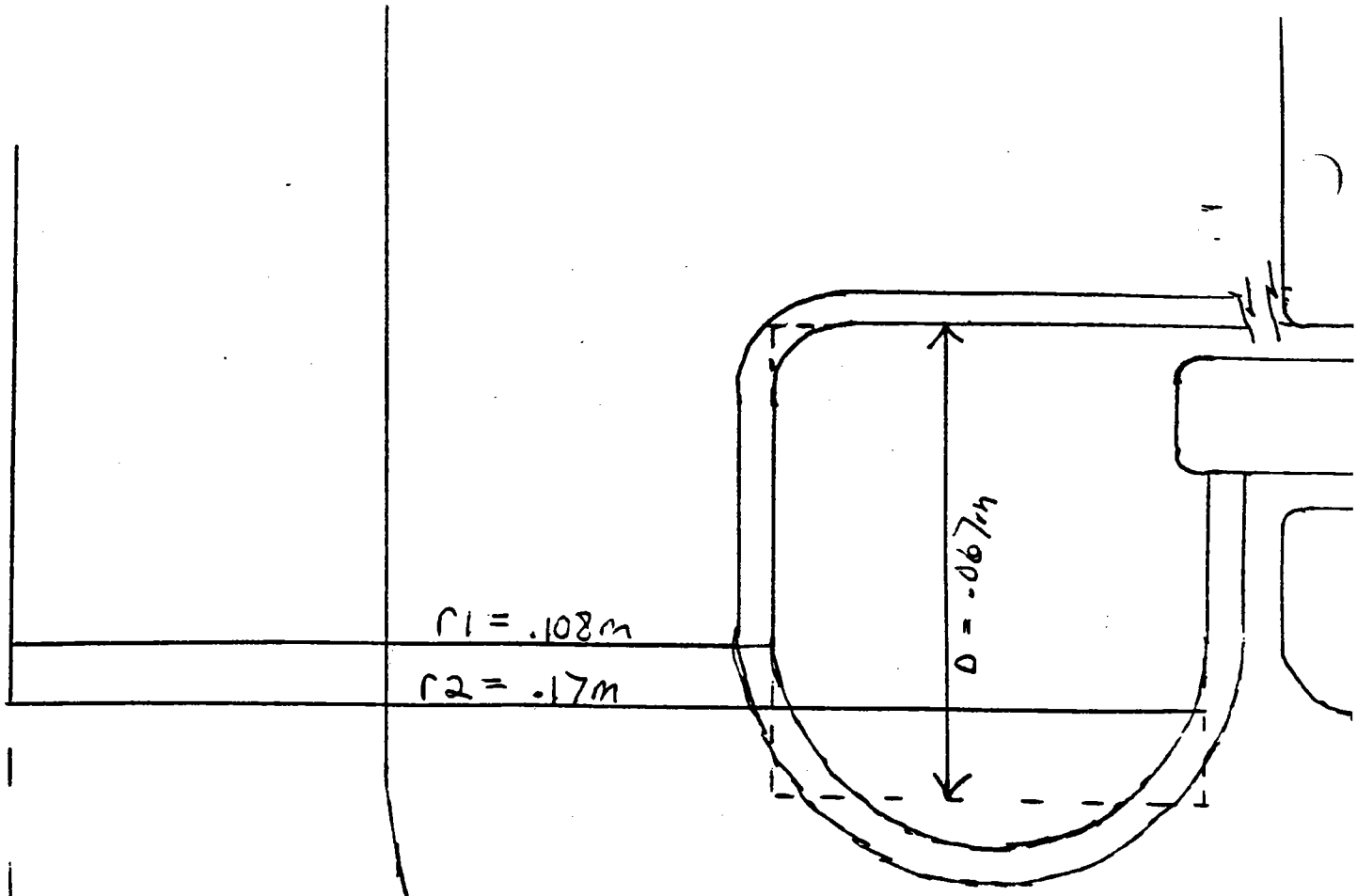
Where θ is the angular change from full coupling. The next table lists the measured loop positions for two differant frequencies. Again, A to C won't neutralize at lower frequencies.

F(Mhz)	θ(A to B)	θ(A to C)
9.310	28.8^{o}	0^{o}
16.094	57.75^{o}	42.52^{o}

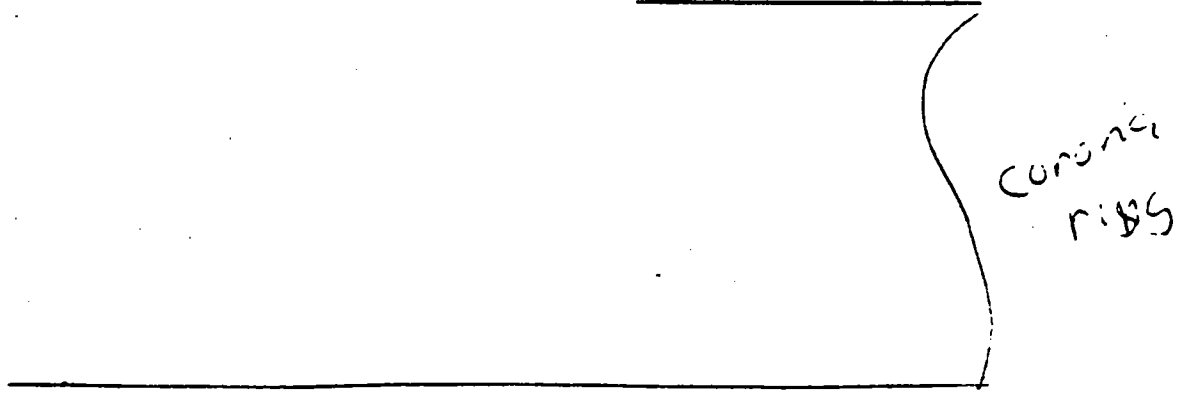
The next table relates the frequency, SF08 current, calculated loop voltage. and measure loop voltage.

F(Mhz)	I(rms)	(A to B) VL (calculated)	(A to C) VL (calculated)	(A to B) VL (measured)	(A to C) VL (measured)
9.310	1260	393	450	400	480
16.094	2100	690	951	720	1050

The numbers all look close enough and pretty consistant. I will take all this at face value with no fudge factors applied. Since the maximum loop voltage error appears to be about 10% I will attempt to yield a design with 10% margin at both ends of the band or greater. The next page has a detail of the present muetralizing loop with the demensions used for the calculations labeled



Current Loop Design



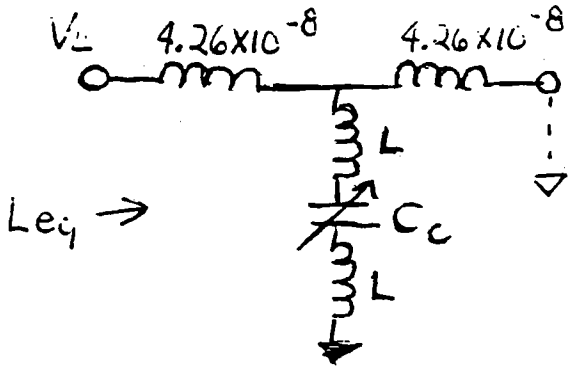
5. Different Neutralizing Schemes

Section 3 has re-designed the loop. Now, instead of changing the loop orientation with respect to the rf magnetic field; we will attempt to nuetralize with a variable capacitance between the two loops. The capacitance may be inserted in series or in shunt. Both approaches will be analysed.

The self inductance of the new loop is about 4.26×10^{-8} Henrys. The following table lists the inductances we need as a function of frequency.

F(Mhz)	L(A to B)	L(A to C)
9.000	1.45×10^{-8}	$.67 \times 10^{-8}$
27.000	8.05×10^{-8}	3.78×10^{-8}

To be able to do this with identical mechanisms requires an inductance tunable from $.67 \times 10^{-8}$ - 10% to 8.05×10^{-8} + 10% The inductance must vary from $.6 \times 10^{-8}$, to 8.9×10^{-8}. This is a 15:1 change! We know this loop is about 4.26×10^{-8} Henrys, and for two loops it is 8.52×10^{-8} Henrys. The first try will be the shunt capacitance variety.



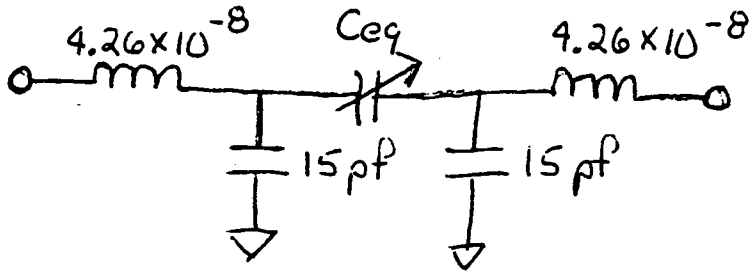
$$Leq = L[1 + 1/(1-\omega^2 LCc)] \qquad Cc = [1 - 1/(Leq/L - 1)](1/\omega^2 L)$$

F	Leq	Cc
9.000	$.6 \times 10^{-8}$	15900pf
27.000	8.9×10^{-8}	67pf

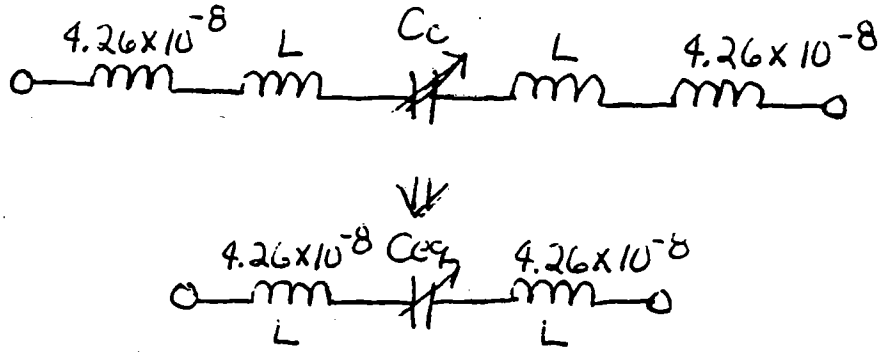
The shunt case is not possible it seems.

a. Series Case

The series case is modeled as:



To greatly simplify the design, I will instead assume the following circuit:



The L's above are inherent in tunable capacitors. The **Ceq** is the net capacitance after adjusting for the L's. The circuitry will be designed in this way. Then the original circuit will be used to fine tune the design using the circuit analysis program Spice.

$$Leq = \frac{Ceq}{2\omega^2 LCeq - 1} \quad -> \quad Ceq = \frac{Leq}{2\omega^2 LLeq - 1}$$

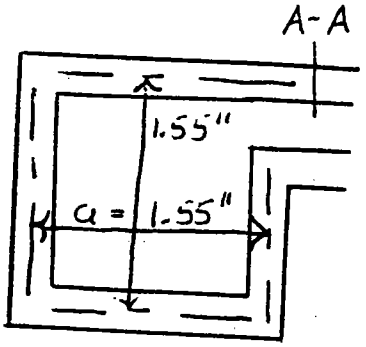
F	Leq	Ceq
9.000	$.6 \times 10^{-8}$	9453×10^{-12}
27.000	8.9×10^{-8}	823×10^{-12}

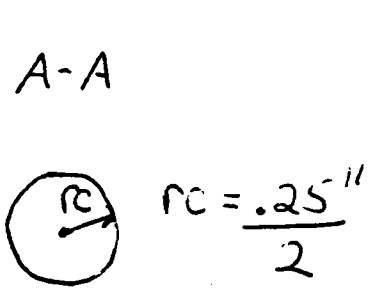
These values are unreasonable, but we can insert a series lumped inductance and decrease them. We need to decrease this value by a factor of 10

F	Leq	Ceq
9.000	$.6 \times 10^{-8}$	945.12pf
27.000	8.9×10^{-8}	90.8pf

The preliminary values above seem reasonable.

Since we need to add inductance, we can make the loops out of 1/4" copper pipe. The demensions would be:



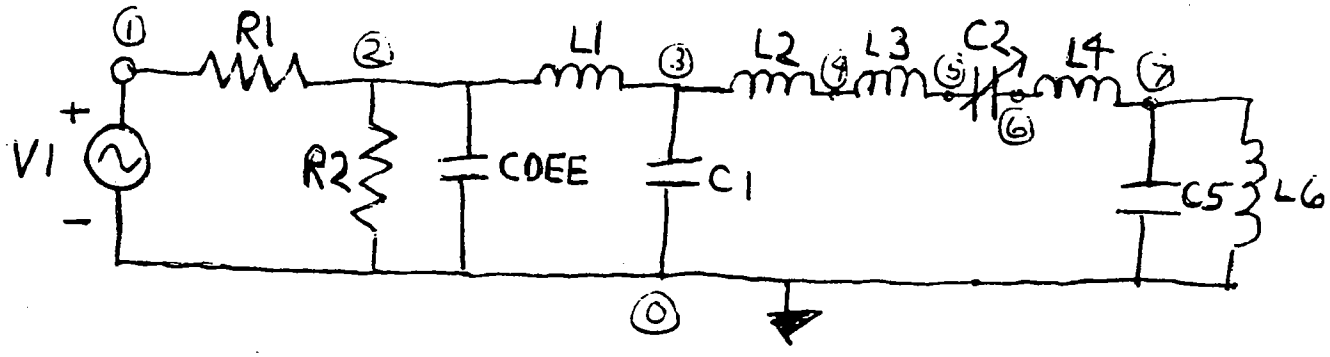


The inductance is:

$$L = (2\mu a/\pi)\ [\ln(a/rc) - .77401] = 5.49 \times 10^{-8}$$

Using this value for L means we must now add .2732μH.

Spice will now be used to fine tune the true circuit. The circuit looks like:



R1 and R2 and V1 are used to excite, the circuit. Cdee is the equivelent dee to dee capacitance transformed up to the loop circuit.

$$Cdee = 1/\omega^2 Leq$$

L1, L6 are the loop inductances of 5.49×10^{-8}H.

L3 and L4 are the stray inductances associated with the variable capacitor (C2) and go as:

$2L = 3.33 \times 10^{-3}C + 15.6)$ nH.

L2 is the added lumped inductance of .2732µh.

C1, C5 are 15pf each due to the connecting transmission line.

C2 is the variable capacitor.

F(Mhz)	Leq(µH)	Cdee(pf)	L3, L4(nH)	C2(cal., pf)	C2(Spice, pf)
9.000	.006	52120	9.41	945.1	790
27.000	.089	390.4	8.49	90.8	111

The descrepancies between C2 calculated and C2 Spice are due to the approximate technique used for hand calculations. It seems apparent that the series tunable capacitor with a lump series inductance is the way to do this. The next four pages are the Spice analysis of the proposed circuit.

* 9MHz Neutralized

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 100
R1 1 2 1E+5
R2 2 0 1E+3
CDEE 2 0 52120E-12
L1 2 3 5.49E-8
C1 3 0 15E-12
L2 3 4 .2732E-6
L3 4 5 9.41E-9
C2 5 6 790E-12
L4 6 7 9.41E-9
C5 7 0 15E-12
L6 7 0 5.49E-8
.AC LIN 30 8.99E+6 9.01E+6
.PLOT AC VM(2,0)
.END
```

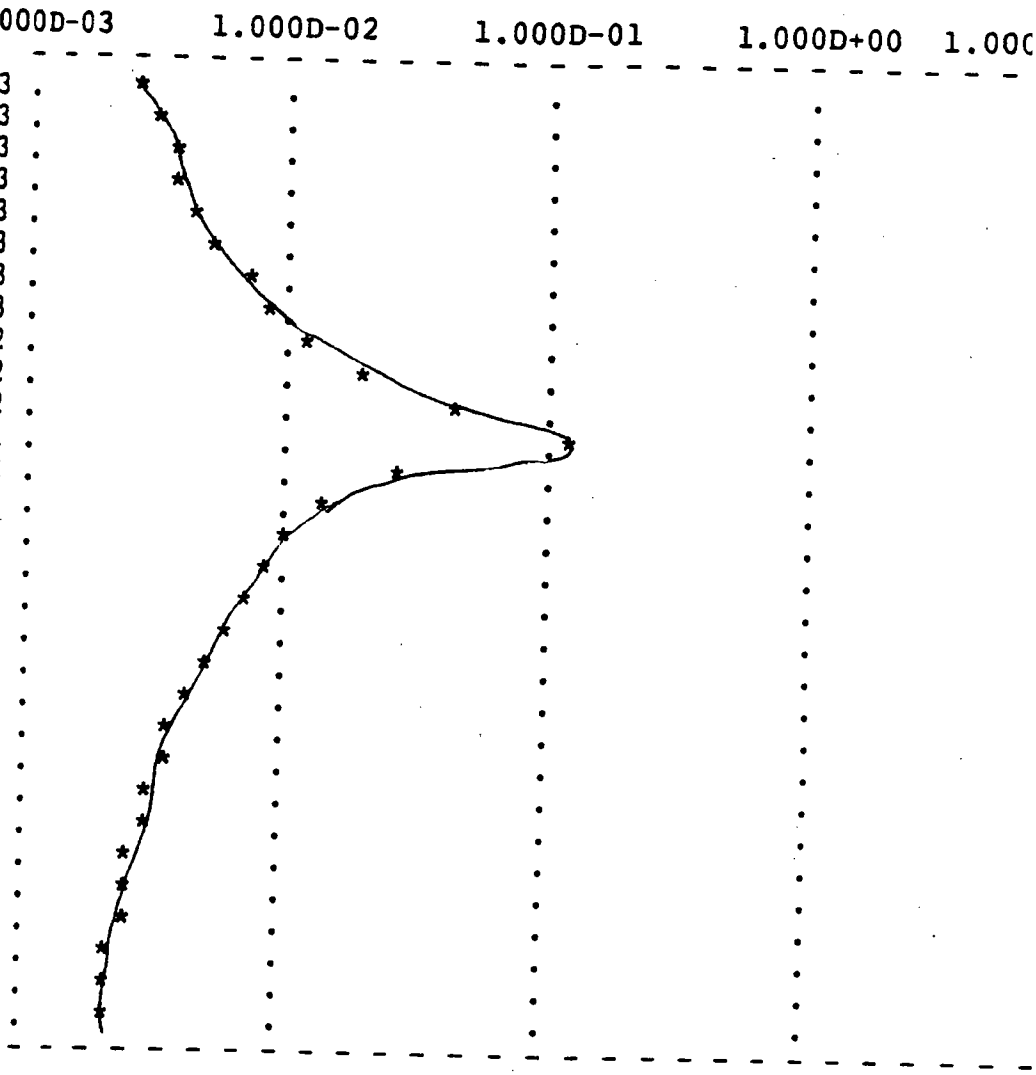
*******24-SEP-85 ******* SPICE 2G.1 (15OCT80) *******13:46:28*****

* 9MHz Neutralizer

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

FREQ	VM(2)
8.990D+06	2.756D-03
8.991D+06	3.074D-03
8.991D+06	3.464D-03
8.992D+06	3.955D-03
8.993D+06	4.593D-03
8.993D+06	5.452D-03
8.994D+06	6.675D-03
8.995D+06	8.552D-03
8.996D+06	1.180D-02
8.996D+06	1.880D-02
8.997D+06	4.483D-02
8.998D+06	1.241D-01
8.998D+06	2.654D-02
8.999D+06	1.498D-02
9.000D+06	1.050D-02
9.000D+06	8.115D-03
9.001D+06	6.637D-03
9.002D+06	5.632D-03
9.002D+06	4.903D-03
9.003D+06	4.350D-03
9.004D+06	3.917D-03
9.004D+06	3.568D-03
9.005D+06	3.281D-03
9.006D+06	3.041D-03
9.007D+06	2.837D-03
9.007D+06	2.661D-03
9.008D+06	2.509D-03
9.009D+06	2.375D-03
9.009D+06	2.257D-03
9.010D+06	2.152D-03



JOB CONCLUDED

TIME CPU	ELAPSED	PAGE FAULTS	DIRECT I/O	BUFFERED I/O
0: 0: 1.44	0: 0: 2.28	250	1	1

* 27 MHz. Neutralizer

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 100
R1 1 2 1E+5
R2 2 0 1E+3
CDEE 2 0 390.4E-12
L1 2 3 5.49E-8
C1 3 0 15E-12
L2 3 4 .2732E-6
L3 4 5 8.49E-9
C2 5 6 111E-12
L4 6 7 8.49E-9
C5 7 0 15E-12
L6 7 0 5.49E-8
.AC LIN 30 26.9E+6 27.1E+6
.PLOT AC VM(2,0)
.END
```

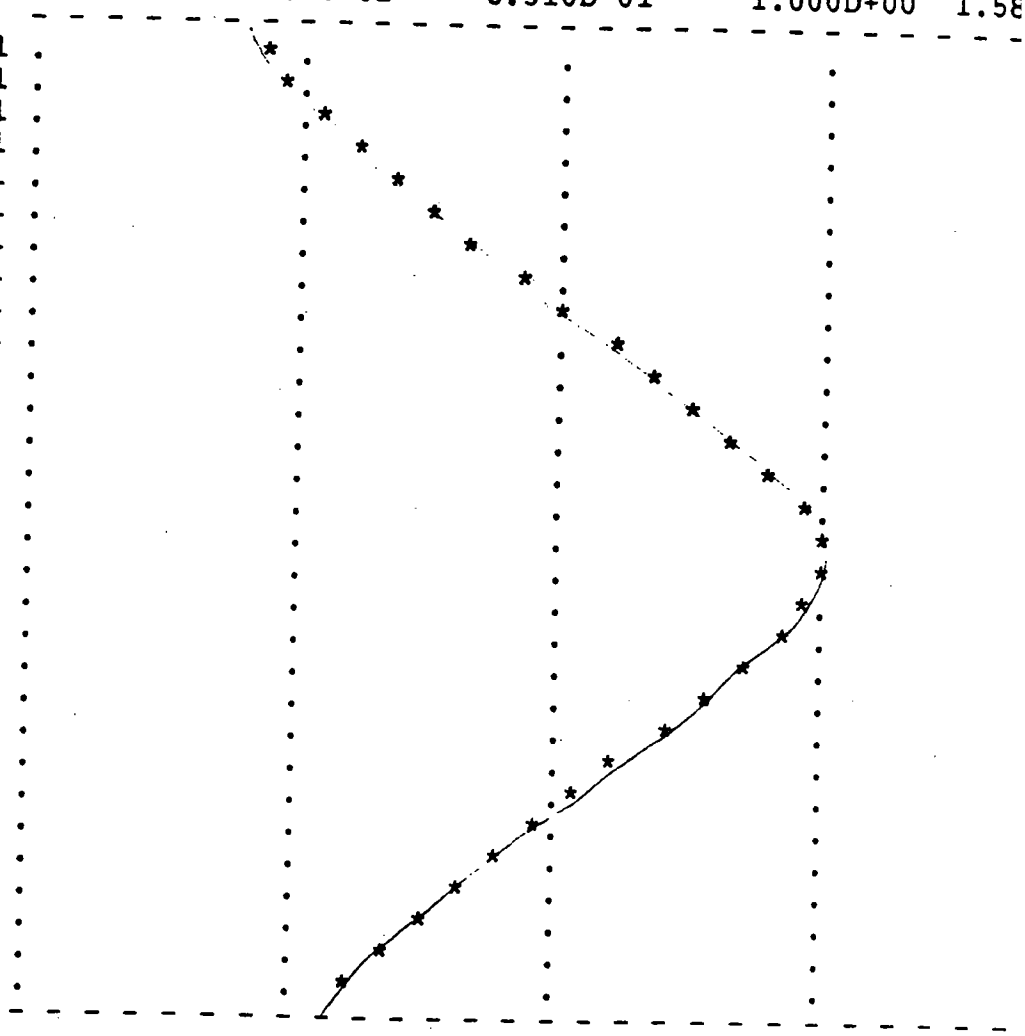
*******24-SEP-85 ******* SPICE 2G.1 (15OCT80) *******13:21:41*****

* 27 MHz Neutralizer

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

FREQ	VM(2)
2.690D+07	3.673D-01
2.691D+07	3.893D-01
2.691D+07	4.138D-01
2.692D+07	4.410D-01
2.693D+07	4.713D-01
2.693D+07	5.053D-01
2.694D+07	5.434D-01
2.695D+07	5.860D-01
2.696D+07	6.334D-01
2.696D+07	6.857D-01
2.697D+07	7.424D-01
2.698D+07	8.021D-01
2.698D+07	8.618D-01
2.699D+07	9.166D-01
2.700D+07	9.602D-01
2.700D+07	9.856D-01
2.701D+07	9.883D-01
2.702D+07	9.679D-01
2.702D+07	9.287D-01
2.703D+07	8.772D-01
2.704D+07	8.200D-01
2.704D+07	7.621D-01
2.705D+07	7.066D-01
2.706D+07	6.552D-01
2.707D+07	6.084D-01
2.707D+07	5.663D-01
2.708D+07	5.285D-01
2.709D+07	4.948D-01
2.709D+07	4.646D-01
2.710D+07	4.375D-01



JOB CONCLUDED

TIME CPU	ELAPSED	PAGE FAULTS	DIRECT I/O	BUFFERED I/O
0: 0: 1.39	0: 0: 2.19	248	1	1

Well, now to burst another bubble, this last circuit is not feasible either.

F	Leq	VL	I
9.000	$.6 \times 10^{-8}$	100	294 amperes!
27.000	3.78×10^{-8}	707	110 amperes!

This current is just plain too high for any reasonably sized comercially available capcitors. Not to mention cooling requirements would be high and if in the future somebody decided to turn it down, the nuetralization would be a function of drive and molten copper!

It is now becoming more and more apparent that we will either allow 2 axes of motion, or use some monstrous huge apparatus, or allow increased loop potentials.

6. Two Axes of Motion

If two axes of motion are allowed, then the loop voltages at lower frequencies can be increased. Again a shunt or series element can be inserted with the value of this element made a mechanical function of the angular loop position. This type of apparatus would not change the operational perception of the nuetralization process, and would allow continued predictions of beginning parameters. If the two elements were independantly tunable, then many different conbinations would be realizable which may lead to unpredicted and possibly dangerous operating conditions

$$VL1 = \mu I_1 F_1 K \qquad 9\ Mhz$$

$$VL2 = \mu I_2 F_2 K \cos\theta \qquad 27 Mhz$$

$$VL1/VL2 = (I_1 F_1)/(I_2 F_2 \cos\theta)$$

If we use the first loop (absolute maximum allowable loop) the loop voltages would be:

F(Mhz)	VL(Vrms)	θ
9.000	303	0
27.000	728	70

If the loop was made out of (1/4) inch pipe and made square the absolute maximum dimensions would be:

$$r2 = 6.625 \text{ inches}$$

$$r1 = 4.875 \text{ inches}$$

$$D = 1.750 \text{ inches}$$

Now:

F(Mhz)	VL(Vrms)	θ
9.000	195	0
27.000	468	70

The self inductance would be:

$$L = 8.12 \times 10^{-8} \text{ Henrys}$$

$$2L = L = 1.62 \times 10^{-7} \text{ Henrys}$$

Shunt Case

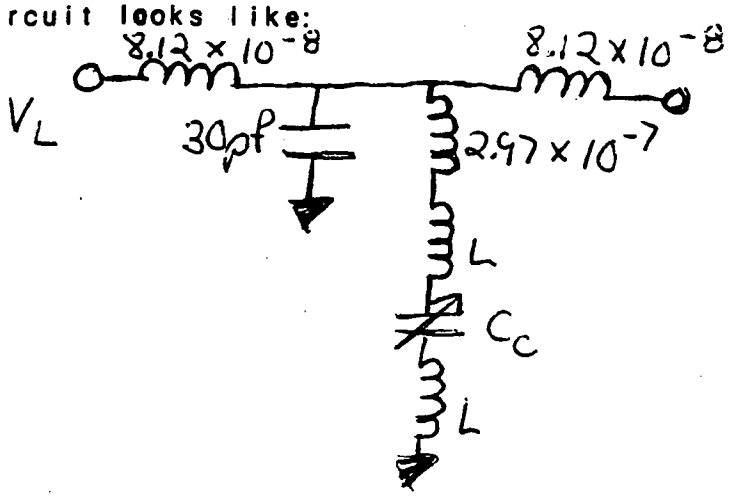
F(Mhz)	Leq	Cc
9.000	2.58×10^{-8}	9496pf
27.000	3.53×10^{-8}	1185pf

Series Case

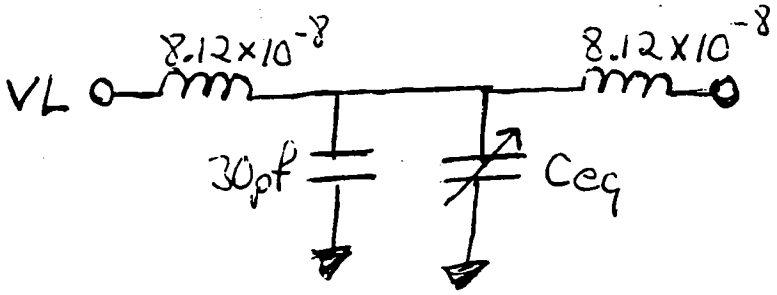
F(Mhz)	Leq	Cc
9.000	2.58×10^{-8}	4527pf
27.000	3.53×10^{-8}	433pf

Neither case looks impossible here. In either case a lumped inductance will have to be added to reduce the necessary variable capacitance values. For the shunt case, we would insert about 2.97×10^{-7} Henrys. For the series case we would insert about 6.26×10^{-7} Henrys. These numbers are too big to get out of the loops alone, so lumped elements would have to be used here. The shunt case will be analysed first.

The circuit looks like:



To evaluate Cc, L is found to be about 8.6325×10^{-9} Henrys. Lumping this value together with 2.97×10^{-7} Henrys and evaluating the equivelent capacitance leaves the following circuit:



$$Ceq = Cc/(1 - \omega^2 LeCc) + 30pf$$

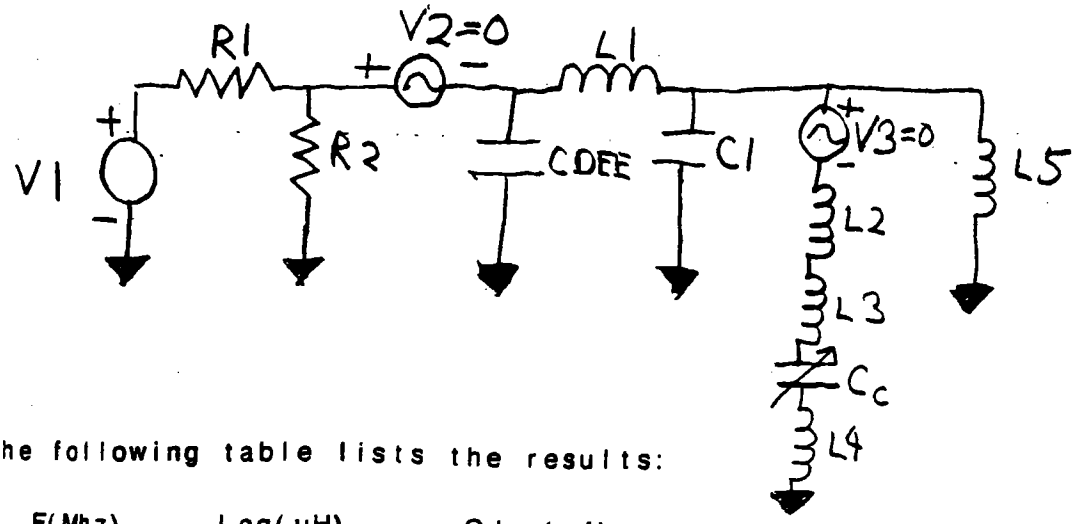
$$Le = 2.97 \times 10^{-7} + 2(8.6325 \times 10^{-9}) \text{ Henrys}$$

$$Ceq = (1/\omega^2 L)[1 - 1/(Leq/L - 1)]$$

Knowing all this, I may now calculate what Cc is. The following table lists the results:

F(Mhz)	Leq(μH)	Ceq(pf)	Cc(pf)
9.000	.0258	9496	900
27.000	.0353	1185	101

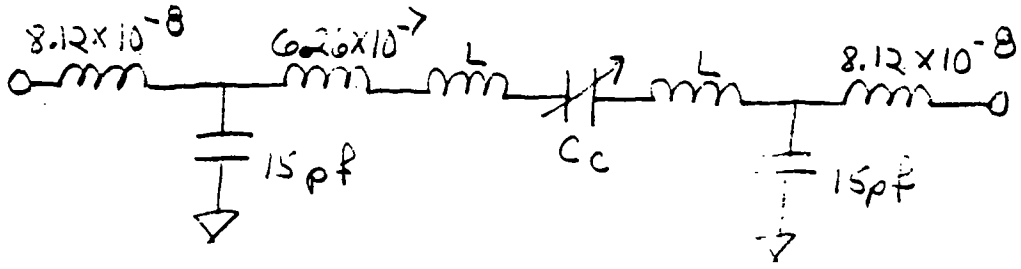
The following circuit is entered into Spice:



The following table lists the results:

F(Mhz)	Leq(μH)	Cdee(pf)	Cc(Spice, pf)	I(Cc)
9.000	.0258	12121	897	241
27.000	.0353	985	100	146

The Spice analysis is included in the next four pages. Again the current is too high for the shunt case. I now turn to the series case. The circuit looks like:



The next table lists the approximate starting values for Cc:

F(Mhz)	Leq(μH)	Ceq(pf)	Cc(pf)
9 000	.0258	4527	453
27 000	.0353	433	43.3

* 9MHz Neutralizer

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 1.95E+6
R1 1 2 10E+6
V2 2 3 AC 0
R2 3 0 10E+3
CDEE 3 0 12121E-12
L1 3 4 8.12E-8
C1 4 0 30E-12
V3 4 6 AC 0
L2 6 7 2.97E-7
L3 7 8 9.3E-9
Cc 8 9 897E-12
L4 9 0 9.3E-9
L5 4 0 8.12E-8
.AC LIN 30 8.99E+6 9.01E+6
.PLOT AC VM(3) I(V3)
.PRINT AC VM(3) I(V3)
.END
```

*******27-SEP-85 ******* SPICE 2G.1 (15OCT80) *******13:43:45*****

* 9 MHz Neutralizer

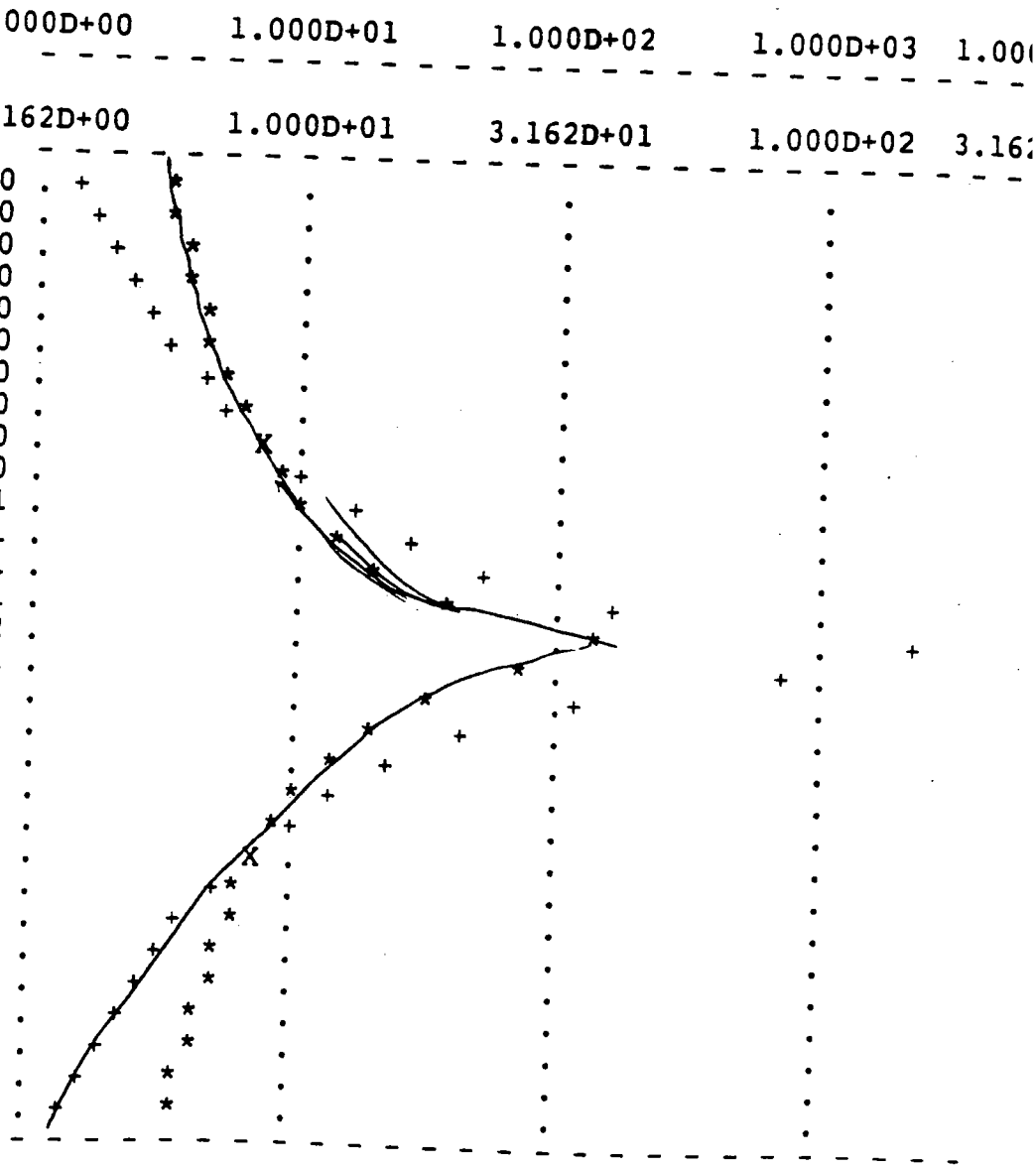
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: VM(3)
+: I(V3)

FREQ	VM(3)
8.990D+06	2.984D+00
8.991D+06	3.232D+00
8.991D+06	3.520D+00
8.992D+06	3.859D+00
8.993D+06	4.264D+00
8.993D+06	4.754D+00
8.994D+06	5.363D+00
8.995D+06	6.137D+00
8.996D+06	7.154D+00
8.996D+06	8.550D+00
8.997D+06	1.059D+01
8.998D+06	1.384D+01
8.998D+06	1.985D+01
8.999D+06	3.470D+01
9.000D+06	1.322D+02
9.000D+06	7.443D+01
9.001D+06	2.931D+01
9.002D+06	1.834D+01
9.002D+06	1.340D+01
9.003D+06	1.058D+01
9.004D+06	8.764D+00
9.004D+06	7.494D+00
9.005D+06	6.556D+00
9.006D+06	5.836D+00
9.007D+06	5.265D+00
9.007D+06	4.801D+00
9.008D+06	4.417D+00
9.009D+06	4.093D+00
9.009D+06	3.818D+00
9.010D+06	3.579D+00



* 27 MHz Neutralizer

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 4.68E+5
R1 1 2 10E+6
V2 2 3 AC 0
R2 3 0 10E+3
CDEE 3 0 985E-12
L1 3 4 8.12E-8
C1 4 0 30E-12
V3 4 6 AC 0
L2 6 7 2.97E-7
L3 7 8 9.3E-9
Cc 8 9 100.5E-12
L4 9 0 9.3E-9
L5 4 0 8.12E-8
.AC LIN 30 26.99E+6 27.01E+6
.PLOT AC VM(3) I(V3)
.PRINT AC VM(3) I(V3)
.END
```

*******27-SEP-85 ******* SPICE 2G.1 (15OCT80) *******13:16:24******

* 27 Megahertz Neutralizer,

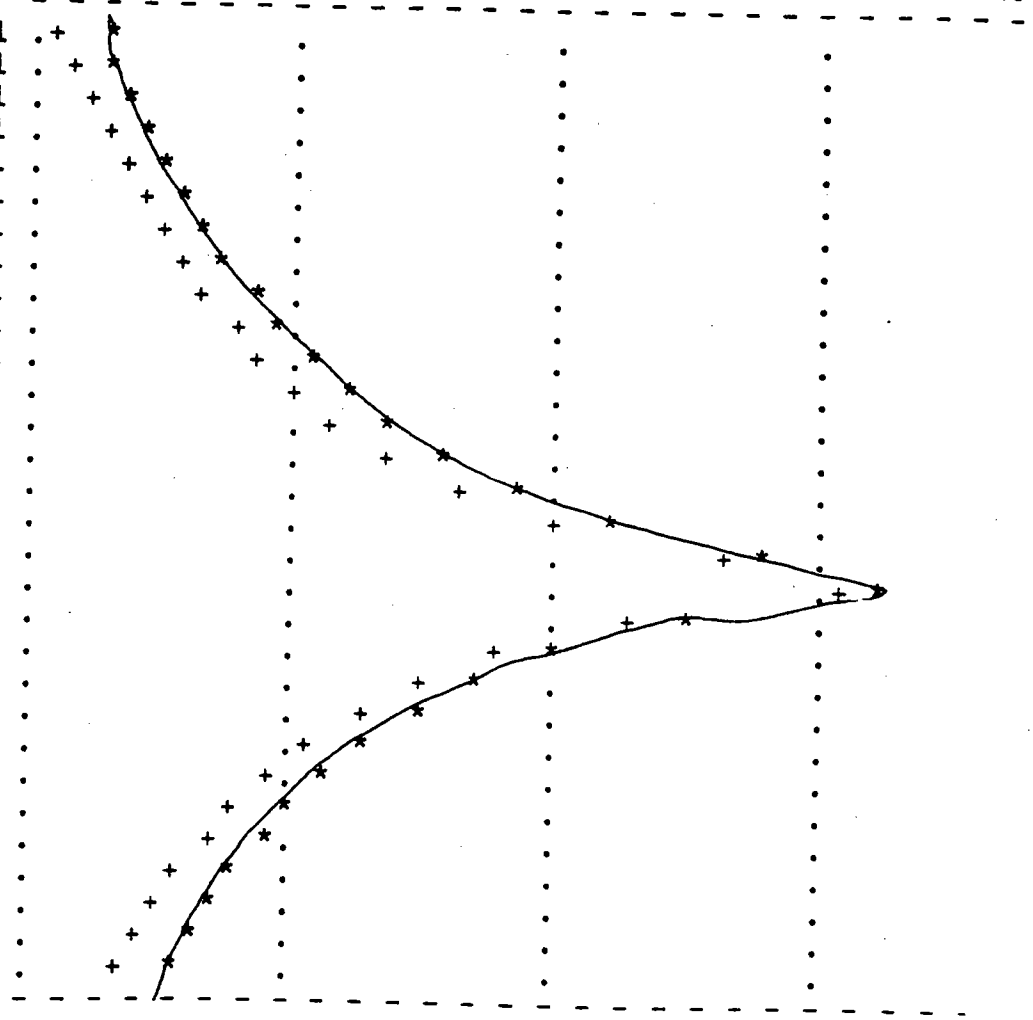
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

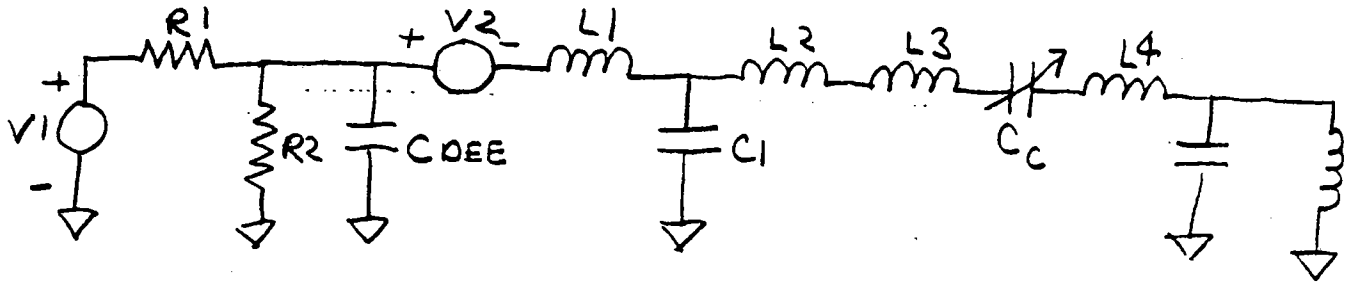
LEGEND:

*: VM(3)
+: I(V3)

FREQ	VM(3)
2.699D+07	1.337D+01
2.699D+07	1.424D+01
2.699D+07	1.522D+01
2.699D+07	1.635D+01
2.699D+07	1.766D+01
2.699D+07	1.919D+01
2.699D+07	2.100D+01
2.699D+07	2.319D+01
2.700D+07	2.587D+01
2.700D+07	2.924D+01
2.700D+07	3.360D+01
2.700D+07	3.947D+01
2.700D+07	4.778D+01
2.700D+07	6.042D+01
2.700D+07	8.194D+01
2.700D+07	1.262D+02
2.700D+07	2.564D+02
2.700D+07	4.160D+02
2.700D+07	1.710D+02
2.700D+07	9.994D+01
2.700D+07	7.015D+01
2.700D+07	5.398D+01
2.701D+07	4.387D+01
2.701D+07	3.695D+01
2.701D+07	3.193D+01
2.701D+07	2.812D+01
2.701D+07	2.512D+01
2.701D+07	2.271D+01
2.701D+07	2.073D+01
2.701D+07	1.907D+01



The following circuit is entered into Spice:



The following table lists the results:

F(Mhz)	Leq(μH)	Cdee(pf)	Cc(pf)	I(Cc)
9.000	.0258	12121	401	133.0
27.000	.0353	985	45	78.2

The Spice analysis is included on the next four pages. The current is now very reasonable. So, this is the first case which appears to be feasible. At 9 Mhz. we only need 50 KVdeepeak, so the current is actually 66.5 amps vs. 133 amps. Somewhere in the operating band there will exist a worst case, I won't pursue it now.

Although the last system would work, it would be desirable to make only one axes tunable and the other an initial installation trimmer. This type of system would be much easier to design and implement while maintaining an ability to adapt to a broader electrical enviornment. Such a system may be realizable with multiple loops and a full 90 degrees of travel. A system could be designed for less than 90 degrees irregardless of system conditions. This would involve two loops with an angular displacement between the two such that at full coupling the potential is roughly double of a single loop and at minimum coupling a bucking action would make the potential zero. This approach although cute, is more difficult so the straight forward double loop approach will be pursued here.

If two of the previouly designed loops were used, then the voltage would double and the self inductance would increase approximately by a factor of four. This leaves 3.248×10^{-7} Henrys per set of loops and $6\ 496 \times 10^{-7}$ Henrys for a complete neutralizing assembly.

******* 3-OCT-85 ******* SPICE 2G.1 (15OCT80) *******10:37:09*****

* 9MHz Near.

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 3.94E+5
R1 1 2 10E+6
R2 2 0 10E+3
CDEE 2 0 12121E-12
V2 2 8 AC 0
L1 8 3 8.12E-8
C1 3 0 15E-12
L2 3 4 6.26E-7
L3 4 5 8.55E-9
Cc 5 6 401E-12
L4 6 7 8.55E-9
L5 7 0 8.12E-8
C2 7 0 15E-12
.AC LIN 30 8.99E+6 9.01E+6
.PLOT AC VM(2) I(V2)
.PRINT AC VM(2) I(V2)
.END
```

******* 3-OCT-85 ******* SPICE 2G.1 (15OCT80) *******10:37:09*****

*

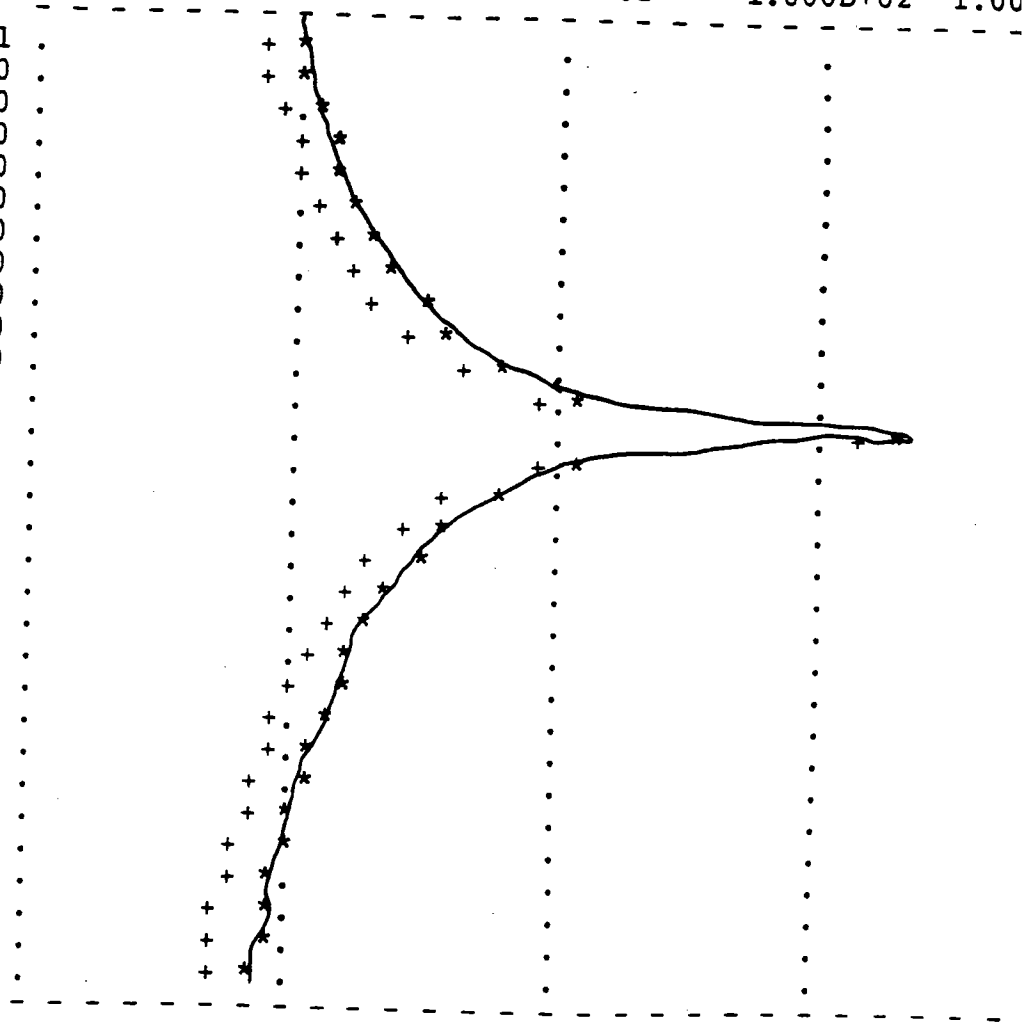
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: VM(2)
+: I(V2)

FREQ	VM(2)
8.990D+06	9.539D-01
8.991D+06	1.046D+00
8.991D+06	1.157D+00
8.992D+06	1.293D+00
8.993D+06	1.462D+00
8.993D+06	1.681D+00
8.994D+06	1.973D+00
8.995D+06	2.383D+00
8.996D+06	3.002D+00
8.996D+06	4.039D+00
8.997D+06	6.143D+00
8.998D+06	1.269D+01
8.998D+06	1.949D+02
8.999D+06	1.150D+01
9.000D+06	5.930D+00
9.000D+06	4.007D+00
9.001D+06	3.032D+00
9.002D+06	2.444D+00
9.002D+06	2.049D+00
9.003D+06	1.767D+00
9.004D+06	1.554D+00
9.004D+06	1.389D+00
9.005D+06	1.256D+00
9.006D+06	1.148D+00
9.007D+06	1.057D+00
9.007D+06	9.803D-01
9.008D+06	9.146D-01
9.009D+06	8.575D-01
9.009D+06	8.076D-01
9.010D+06	7.635D-01



JOB CONCLUDED

* 27 MHz. Nec'd.

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 5.6545E+5
R1 1 2 10E+6
R2 2 0 10E+3
CDEE 2 0 985E-12
V2 2 8 AC 0
L1 8 3 8.12E-8
C1 3 0 15E-12
L2 3 4 6.26E-7
L3 4 5 7.88E-9
Cc 5 6 44.95E-12
L4 6 7 7.88E-9
L5 7 0 8.12E-8
C2 7 0 15E-12
.AC LIN 30 26.99E+6 27.01E+6
.PLOT AC VM(2) I(V2)
.PRINT AC VM(2) I(V2)
.END
```

******* 3-OCT-85 ******* SPICE 2G.1 (15OCT80) *******10:56:09*****

*

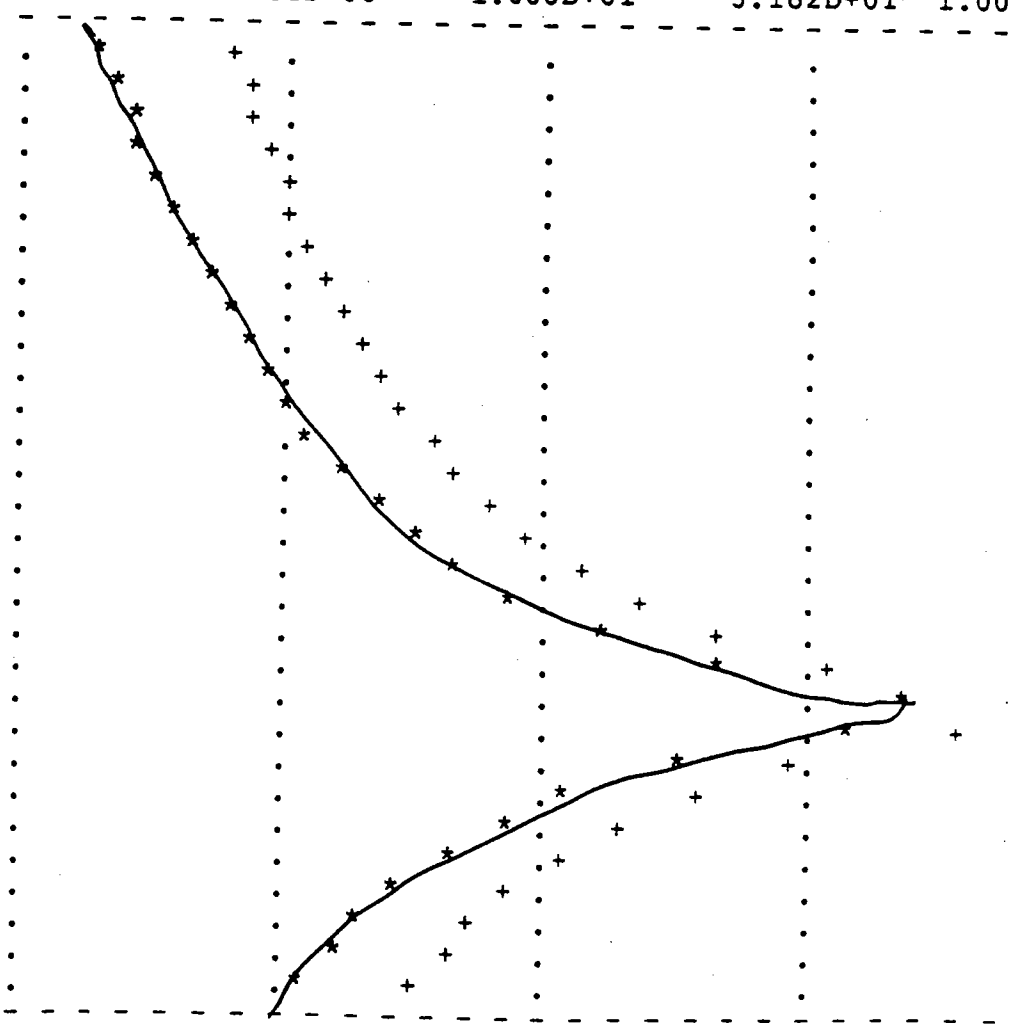
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

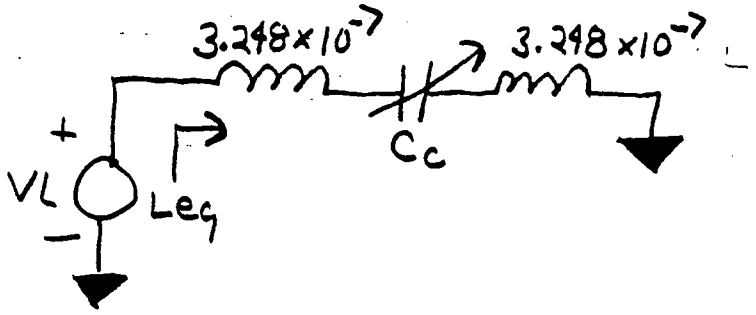
*: VM(2)
+: I(V2)

FREQ	VM(2)
2.699D+07	1.435D+01
2.699D+07	1.511D+01
2.699D+07	1.595D+01
2.699D+07	1.689D+01
2.699D+07	1.794D+01
2.699D+07	1.913D+01
2.699D+07	2.048D+01
2.699D+07	2.204D+01
2.700D+07	2.384D+01
2.700D+07	2.597D+01
2.700D+07	2.850D+01
2.700D+07	3.157D+01
2.700D+07	3.537D+01
2.700D+07	4.020D+01
2.700D+07	4.653D+01
2.700D+07	5.520D+01
2.700D+07	6.778D+01
2.700D+07	8.763D+01
2.700D+07	1.234D+02
2.700D+07	2.049D+02
2.700D+07	4.681D+02
2.700D+07	3.592D+02
2.701D+07	1.735D+02
2.701D+07	1.112D+02
2.701D+07	8.151D+01
2.701D+07	6.428D+01
2.701D+07	5.306D+01
2.701D+07	4.517D+01
2.701D+07	3.934D+01
2.701D+07	3.484D+01



The Series Trimmer approach:

The following circuit will be analysed:



$$Leq = L - (1/\omega)^2 (1/Cc) = (4/Cdee)[VL/(Vdee\omega)]^2$$

At F = 9 Mhz., VL = 390 Volts therefore;

Cc = 729 pf for Cdee = .0863 pf

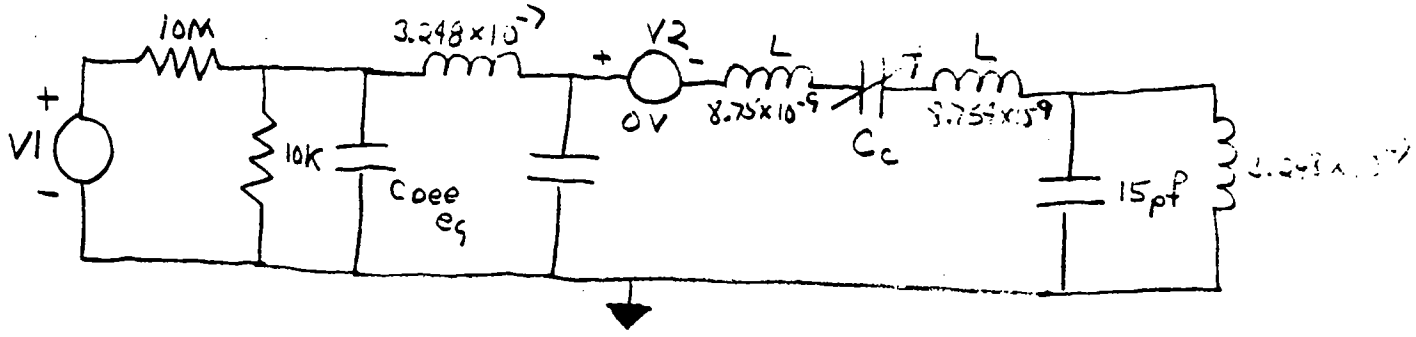
Cc = 573 pf for Cdee = .184 pf

This leaves the following operating conditions for 27 Mhz.:

VL = 1538 Volts rms for Cdee = .0863 pf

VL = 2822 Volts rms for Cdee = .184 pf

So it appears if we allow loop tolerances for upwards of 3500 Volts rms then we may have another solution. The spice analysis for the following circuit appears on the next four pages.



* 9 MHz Near.

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 2.8346E+6
R1 1 2 10E+6
R2 2 0 10E+3
CDEE 2 0 6048E-12
L1 2 3 3.248E-7
C1 3 0 15E-12
V2 3 4 AC 0
L2 4 5 8.75E-9
Cc 5 6 500E-12
L3 6 7 8.754E-9
C2 7 0 15E-12
L4 7 0 3.248E-7
.AC LIN 30 8.99E+6 9.02E+6
.PLOT AC VM(2) I(V2)
.PRINT AC VM(2) I(V2)
.END
```

*******15-OCT-85 ******* SPICE 2G.1 (15OCT80) *******16:04:10*****

*

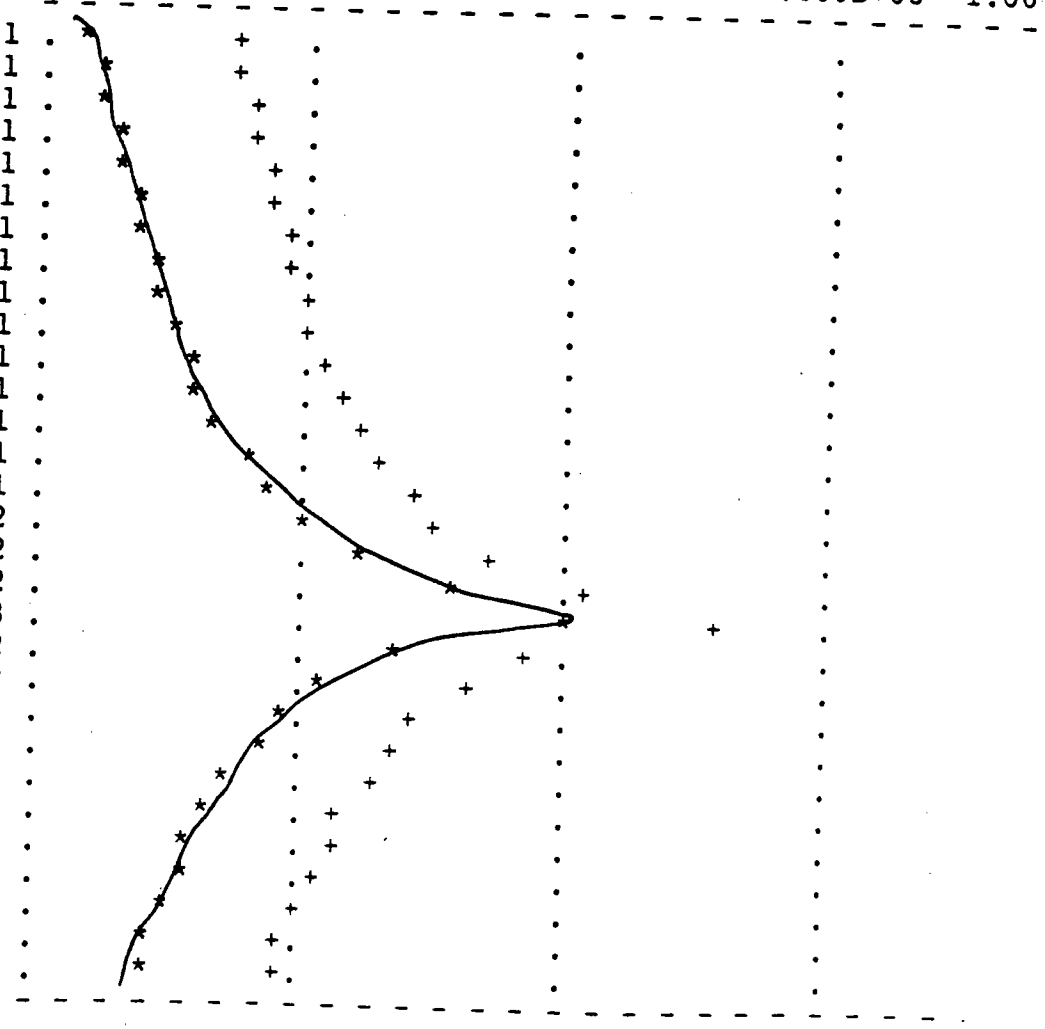
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: VM(2)
+: I(V2)

FREQ	VM(2)
8.990D+06	1.490D+01
8.991D+06	1.584D+01
8.992D+06	1.689D+01
8.993D+06	1.809D+01
8.994D+06	1.946D+01
8.995D+06	2.105D+01
8.996D+06	2.290D+01
8.997D+06	2.511D+01
8.998D+06	2.776D+01
8.999D+06	3.102D+01
9.000D+06	3.512D+01
9.001D+06	4.043D+01
9.002D+06	4.759D+01
9.003D+06	5.775D+01
9.004D+06	7.333D+01
9.006D+06	1.002D+02
9.007D+06	1.575D+02
9.008D+06	3.644D+02
9.009D+06	1.059D+03
9.010D+06	2.239D+02
9.011D+06	1.247D+02
9.012D+06	8.657D+01
9.013D+06	6.637D+01
9.014D+06	5.386D+01
9.015D+06	4.536D+01
9.016D+06	3.921D+01
9.017D+06	3.455D+01
9.018D+06	3.090D+01
9.019D+06	2.796D+01
9.020D+06	2.554D+01



* 27 MHz. Net

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

****

```
.WIDTH IN=80 OUT=60
V1 1 0 AC 2.8346E+6
R1 1 2 10E+6
R2 2 0 10E+3
CDEE 2 0 49E-12
L1 2 3 3.248E-7
C1 3 0 15E-12
V2 3 4 AC 0
L2 4 5 8.75E-9
Cc 5 6 500E-12
L3 6 7 8.754E-9
C2 7 0 15E-12
L4 7 0 3.248E-7
.AC LIN 30 26.5E+6 27.5E+6
.PLOT AC VM(2) I(V2)
.PRINT AC VM(2) I(V2)
.END
```

*******15-OCT-85 ******* SPICE 2G.1 (15OCT80) *******16:10:09*****

*

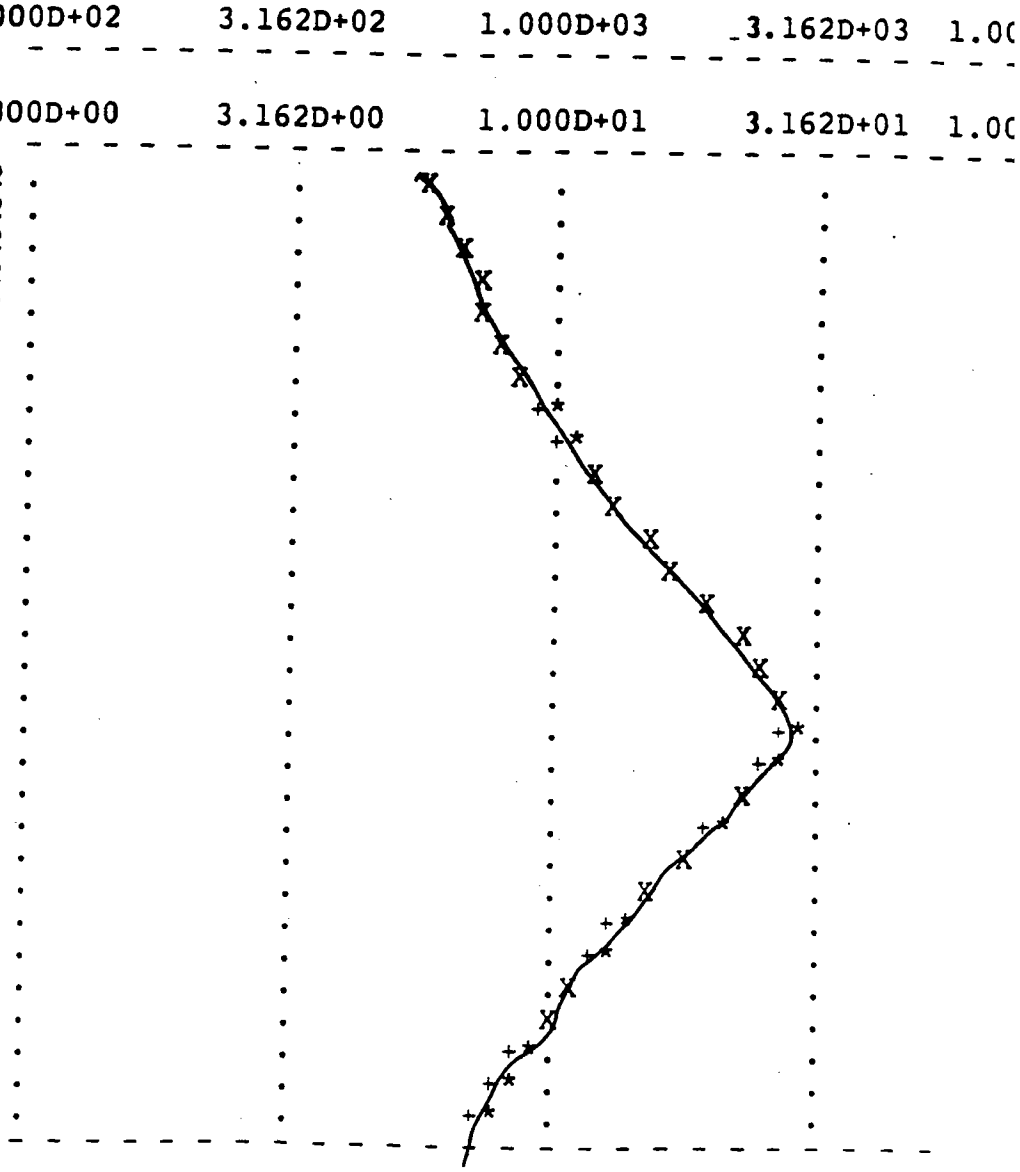
**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

****

LEGEND:

*: VM(2)
+: I(V2)

FREQ	VM(2)
2.650D+07	5.763D+02
2.653D+07	6.120D+02
2.657D+07	6.521D+02
2.660D+07	6.976D+02
2.664D+07	7.496D+02
2.667D+07	8.095D+02
2.671D+07	8.792D+02
2.674D+07	9.609D+02
2.678D+07	1.058D+03
2.681D+07	1.174D+03
2.684D+07	1.316D+03
2.688D+07	1.488D+03
2.691D+07	1.701D+03
2.695D+07	1.958D+03
2.698D+07	2.256D+03
2.702D+07	2.560D+03
2.705D+07	2.783D+03
2.709D+07	2.819D+03
2.712D+07	2.646D+03
2.716D+07	2.359D+03
2.719D+07	2.055D+03
2.722D+07	1.786D+03
2.726D+07	1.562D+03
2.729D+07	1.378D+03
2.733D+07	1.229D+03
2.736D+07	1.106D+03
2.740D+07	1.004D+03
2.743D+07	9.184D+02
2.747D+07	8.455D+02
2.750D+07	7.830D+02



The following table lists the results:

F(Mhz)	Cc(A to B)	Cc(A to C)	VL(A to B)	VL(A to C)	I(Cc)
9.000	637	500	390	390	131.7
27.000	637	500	1000	3064	29.8

VL(A to B) and Cc(A to B) are estimated from A to C variations. I(Cc) is the worst case value. It appears this case is also a possibility if higher loop voltages are designed for. The shunt trimmer case was also considered but did not pan out well.

6. Conclusion.

Various cases were considered for possible improved neutralizing conditions. Only two of those considered seem to be applicable. These are:

a. A single loop with a fixed lumped inductance and a variable capacitive reactance inserted in series. The capacitive reactance is a mechanical function of loop angle for purposes of operational safety and repeatability.

b. Two loops with a variable capacitive reactance inserted in series. The capacitor is trimmed during initial installation (and on any necessary occasions therafter) then remains fixed.

Pros and Cons

Option a.

Pros:

1. Uses low loop voltages.

Cons:

1. Is mechanically complex.
2. Uses two lumped elements.

Option b.

Pros:

1. Is mechanically simpler.
2. Uses one lumped element.

Cons:

1. Requires higher loop voltages.

Both of these designs appear to be workable, I perfer option b. I can't garantee either of these will work first time, but what is used now is very similar so the odds are good. We should pick a design, mechanically design and build it, and try it on the K500.

Other ways of neutralizing exist such as deriving signals by capacitively coupling to the dees. I believe Texas A&M and Milan's accelarators will be trying this way. I am leary of attempting such methods from experience with our input coupling capacitors. Multipactoring and related phenomena due to insulator to metal joints are problems waiting to be had. But. this method would make the upper dee shells symetric to the lowers which is probably a big plus for the attempt. I will write another note describing the design choosen(if one is) in detail along with initial setup, calibration, and test procedures.